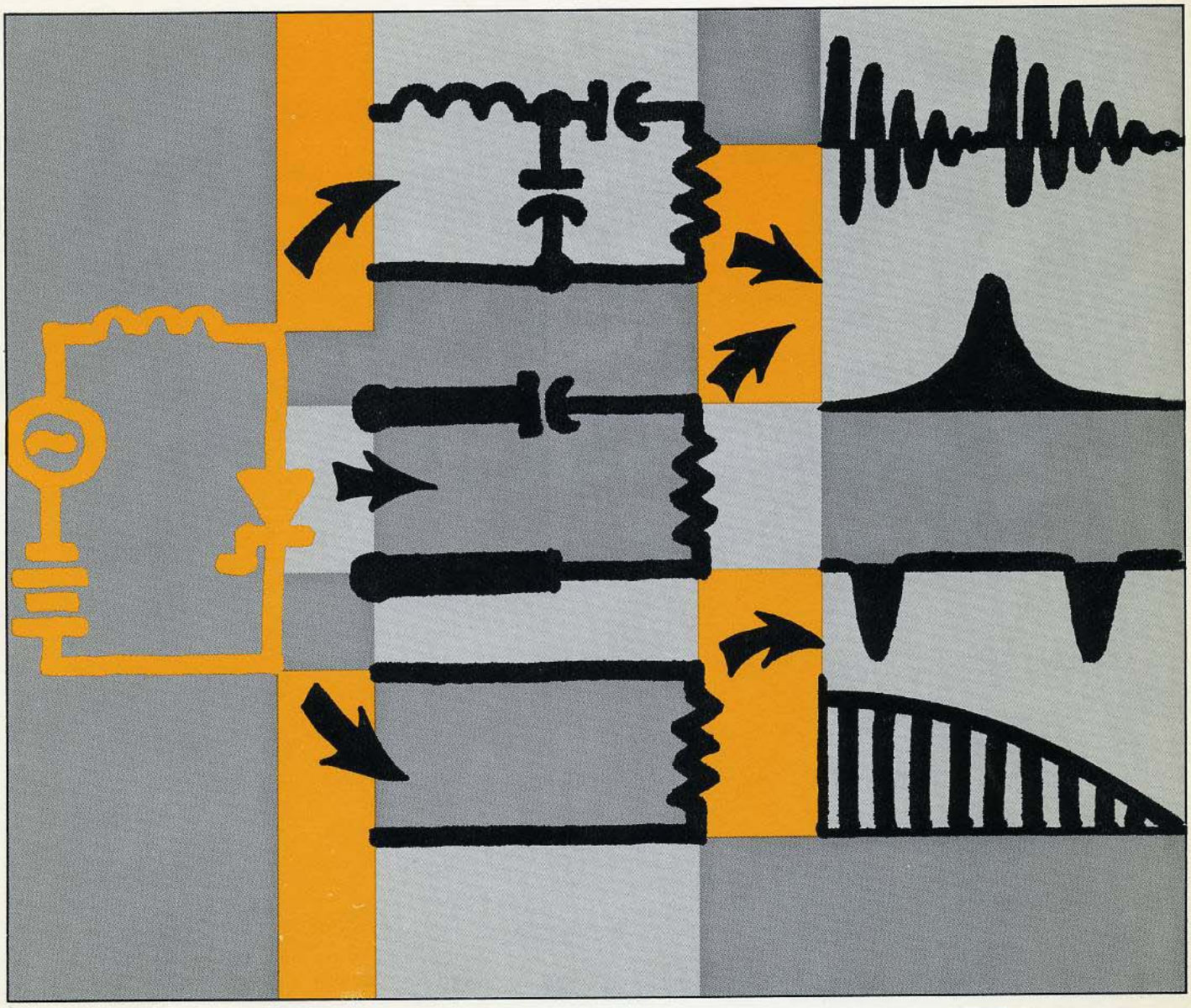
APPLICATION NOTE 920

HARMONIC GENERATION
USING STEP RECOVERY DIODES AND SRD MODULES



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I. Introduction

Since its commercial introduction by HP four years ago, the Step Recovery Diode (SRD) has found many useful applications. Two major applications are in Harmonic Frequency Multiplication and "Comb" Spectrum Generation, which are the topics of this note. The other is in pulse generation and shaping, which is the subject of HP AN918.

SRD frequency multipliers differ considerably from the generally familiar varactor multipliers. The varactor multiplier can be classed as a Variable Reactance Multiplier (VRM) since it is the non-linear, reverse-bias capacitance variation of the varactor which is employed as the principal mechanism for generating the desired harmonics. By contrast, the SRD multiplier can be viewed as a Switching Reactance Multiplier (SRM) since its operation is based on the SRD having two discrete states of reactance and on its ability to switch rapidly between these two states. The two states of reactance, which correspond to high capacitance when the diode is forward biased and low capacitance when it is reverse biased, permit us to consider the SRD as a simple, and efficient, charge-controlled switch.

During the past three years, this mode of frequency multiplication has been extensively studied at HP and elsewhere.[1–14] The general conclusion is that extremely simple, efficient, stable, and broadband high-order multipliers can be built routinely in the frequency range of tens of megahertz to tens of gigahertz.

This note describes the fundamental theoretical considerations and practical design techniques which have been found useful in the design of switching reactance multipliers, and illustrates many practical multiplier designs. Illustrations include the use of conventionally packaged SRD's imbedded in the familiar lumped or distributed-parameter circuits, and the use of modular, hybrid-integrated SRD circuits. This latter approach offers many advantages over conventional circuit techniques, particularly at higher frequencies or multiplication ratios where the diode and circuit interaction become extremely critical and require very precise control.

These advantages have led to the creation of a new commercial line of HP frequency multiplier and frequency "comb" generator modules. The characteristics and application of these hybrid-integrated modules are also described, giving the user a broad choice of design approaches from which to select the one most suited to his end use.

Finally, the note summarizes some important design criteria concerning multiplier Noise, Bandwidth, and Stability, and describes conditions and criteria leading to multipliers that are stable over a broad temperature range and under all phases of short circuit termination.

II. Switching Reactance Multiplier (SRM)

1. General Description

A block diagram of a typical SRM and the waveforms generated at each stage are shown in Figure 1.

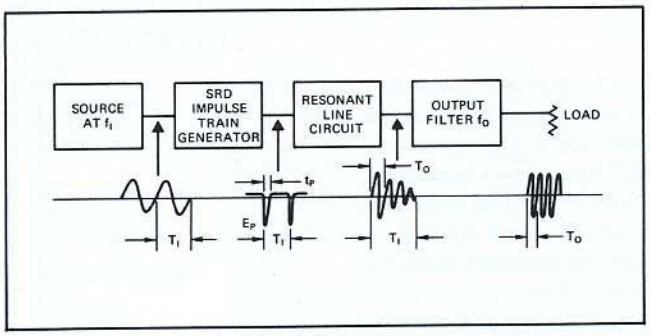


Figure 1. Typical Switching Reactance Multiplier

The signal source, at frequency f_i, delivers energy to a Step Recovery Diode "Impulse Generator" circuit. This circuit converts the energy in each input cycle into a narrow, large amplitude, voltage pulse that occurs once per input cycle. The energy in this pulse is used to shock excite an output resonant circuit, having a loaded $Q \approx \pi/2\,n$. This resonant circuit converts the impulse into a damped ringing waveform at the output frequency, $f_o = n f_i$. This energy is then filtered and delivered to the load as essentially pure CW at the output frequency.

For this process to occur efficiently, the width, t_p, of the pulse formed across the diode should be less than a period of the output frequency ($t_p < 1/f_o$). Step recovery diodes capable of producing such pulses are available for output frequencies up to about 18 GHz.

2. Principle of Operation

a) Diode Behavior: The SRD is assumed to be driven hard into forward, then hard into reverse. Both in forward and reverse, its equivalent circuit is a capacitor as shown in Figure 2. For simplicity at this point, it is assumed that switching from C_{Fwd} to C_{VR} occurs in zero time.

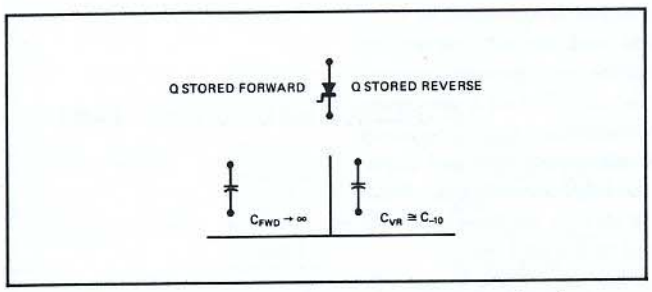


Figure 2. Simplified SRD Equivalent Circuit

b) Impulse Train Generator: The diode is embedded in the network of Figure 3. This network forms the high amplitude, narrow "impulse," once per input cycle (see Ref. 1) by storing energy in a "driving inductance," L, just prior to the diode capacitance switching from C_{Fwd} to C_{VR}. The energy stored in this inductance is $(1/2\ LI_p'^2)$*. This energy appears across C_{VR} after switching, as half-sine pulse with a height E_p', and width t_p'.

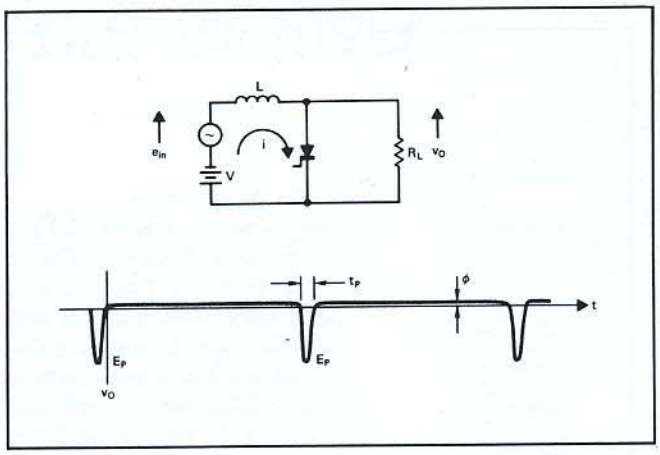


Figure 3. Simplified Impulse Train Generator Circuit

If the energy in this impulse were the same as was stored in the inductance (light loading on the LC circuit) then:

$$\frac{1}{2} I_p'^2 L \cong \frac{1}{2} C_{VR} E_p'^2$$

and $$E_p' \cong I_p' \sqrt{L/C_{VR}}$$

The impulse width t_p' is determined by the resonance frequency of the LC circuit and is:

$$t_p' \cong \pi\sqrt{LC_{VR}}$$

Increasing the loading (by lowering R_L) reduces the impulse height E_p' and increases the impulse width, t_p'.

The loaded impulse height becomes:

$$E_p = E_p' \exp \frac{-\pi\zeta}{2\sqrt{1-\zeta^2}}$$

And the loaded impulse width becomes:

$$t_p = \frac{\pi\sqrt{LC_{VR}}}{\sqrt{1-\zeta^2}}$$

In both of the above ζ is the damping factor which is related to the circuit parameters as:

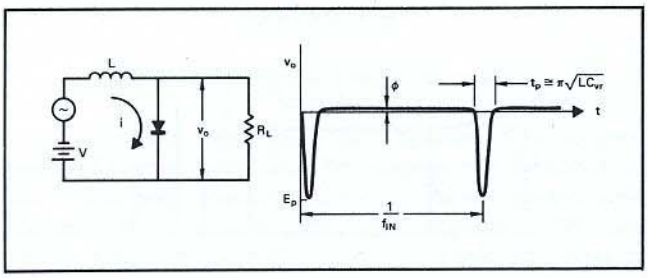
$$\zeta = \frac{1}{2R_L}\sqrt{\frac{L}{C_{VR}}}$$

The power in the impulse train will be given (for $\zeta \ll 1$) by:

$$P_{impulse\ train} = \frac{\pi\zeta E_p^2 f_i C_{VR}}{\sqrt{1-\zeta^2}} \cong \pi\zeta E_p^2 f_i C_{vr}$$

The pulse train, of Figure 3, may be represented by an equivalent generator, based on the Fourier Series description of the waveform (Figure 4).

*Where I_p' is the peak extraction current flowing through L and the diode at the instant the charge goes to zero in the I-layer.



"Impulse Generator Output Voltage"
Time Domain

$v_o \cong E \sin N\,\omega t\}$ for $t = o$ to $t = t_p$

$v_0 = \phi\}$ for $t = t_p$ to $t = 1/f_i$

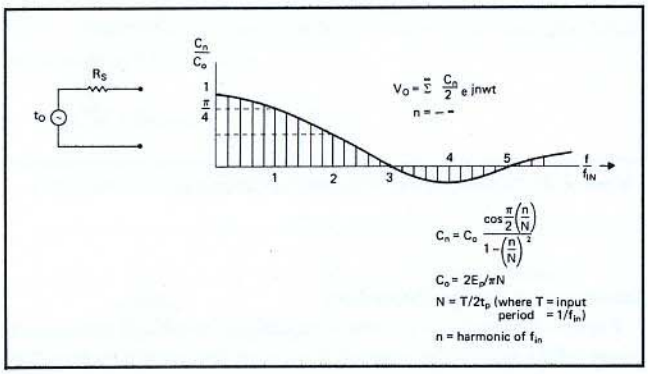


Figure 4. The Impulse Waveform and Its Fourier Spectrum

The line spectrum has its first zero at $f = 3/2t_p$ (assuming a sinusoidal pulse). The "flatness" of the line spectrum between any two arbitrary lines is determined by the pulse width; the narrower the pulse, the higher the first "zero crossing"; in the limit, if it were physically possible, zero pulse width would correspond to a flat amplitude line spectrum to $f = \infty$. The narrowest pulses produced to date in practice have been $t_p \approx 70$ picoseconds (using hybrid integrated modules as discussed in Section IV).

The pulse train of Figures 3 and 4 is of use in itself as a "comb" generating device, producing a line at each multiple of f_i, for system amplitude and frequency calibration, phase locking systems, and reference frequency production. It is also the **key** element in a CW multiplier. The pulse width, in CW multiplier applications, is set in the range:

$$\frac{1}{2f_0} < t_p < \frac{1}{f_0}$$

where $f_0 = n f_i$

The "impulse" is fed into an appropriate resonant output network (as opposed to the resistive load used in "comb" generation). The loaded Q of the resonant network is adjusted to be approximately equal to $\pi/2\,n$, so that most of the energy in the impulse is delivered in a time equal to n cycles of the output frequency (or one cycle of the input frequency). In this way, most of the energy in the impulse ($\approx 1/2\,E_p{}^2\,C_{VR}$) will be delivered at $n f_i = f_o$.

Several types of resonant output networks that have been used are discussed below.

The Resonant Network

When the SRD impulse generator is terminated in a broadband, resistance load, the output is the impulse train waveform and its associated comb spectrum. When terminated in a resonant network (Figure 5), the output ideally has the same energy but now is concentrated around $f_0 = n f_i$.

Three different types of possible resonant output networks are shown in Figure 6. Each of these networks produces the required damped waveform voltage of Figure 5 in which most* of the energy of the impulse has been concentrated in the vicinity of $n f_i = f_o$.

This resonant network may be viewed as the first section of the output filter of the multiplier. Additional sections are added to provide better rejection of the adjacent sidebands $n-1$ and $n+1$.

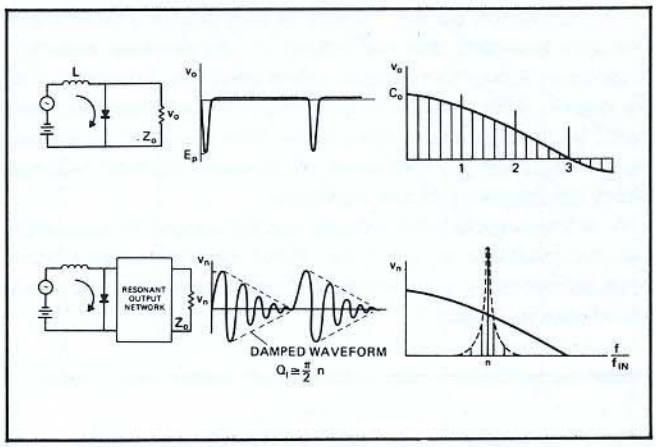


Figure 5

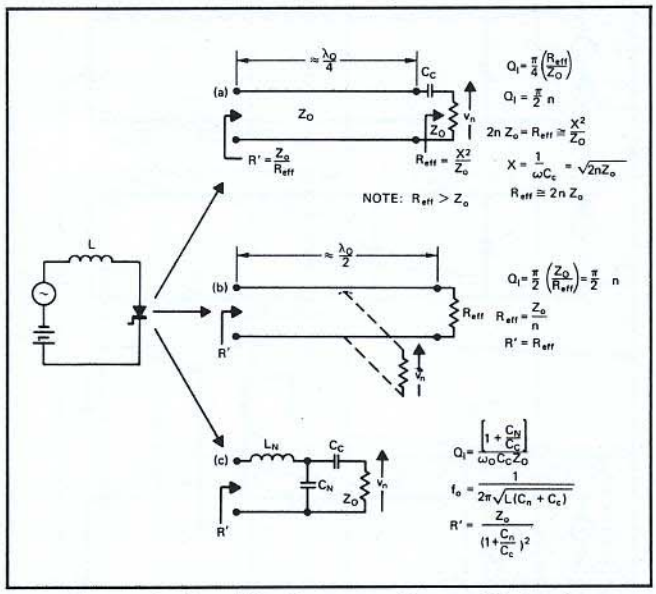


Figure 6. Possible Resonant Output Networks

*For $Q_l = \pi/2\,n$, 76% of the impulse energy is in the $n f_i$ line. This assumes that the R_s of the diode is zero. R_x loss may be accounted for as a perturbation.

Final Filtering

The output of the resonant network, Figure 5, still contains relatively high level sidebands at $n-1$ and $n+1$. These sidebands must be reduced in practical multipliers by further filtering. The resonant network examples of Figure 6 provide flexible means for coupling into various filter types. Examples Figure 6a and 6c are intended for E-field coupling to filters: Figure 6b is for H-field coupling. The distinction between E and H field coupling is drawn more clearly in Figure 8 in which some examples of complete multiplier prototypes of each type are given. In each case, the design procedure for the output network is basically the same: the filter design is pursued independently in a 50 Ω system—i.e., 50 Ω generator and 50 Ω load; the design of the damped waveform circuit is optimized into a 50 Ω load; the filter and the damped waveform generator are married together to give an overall CW multiplier.

The limitation on the validity of this design procedure is that it is assumed that the output of the resonant network behaves as a resistive source. It has variation, however, that we ignore. This is not troublesome provided that the fractional bandwidth of the filter is less than $1/n$ ($bw/f_o << 1/n$). In this case, the Q variation of the resonant network will not affect the response of the multiplier.

A more general filter design for the output is desirable, but not available at this time. Filter prototypes that have been successfully used with the damped waveform network are shown in Figure 9.

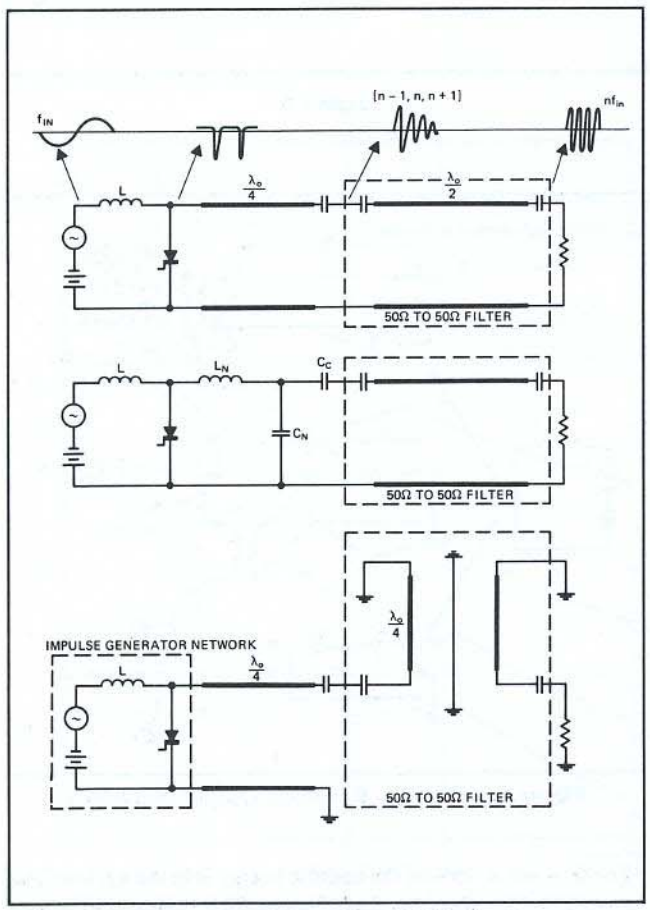


Figure 7. Examples of Complete Multiplier Prototypes

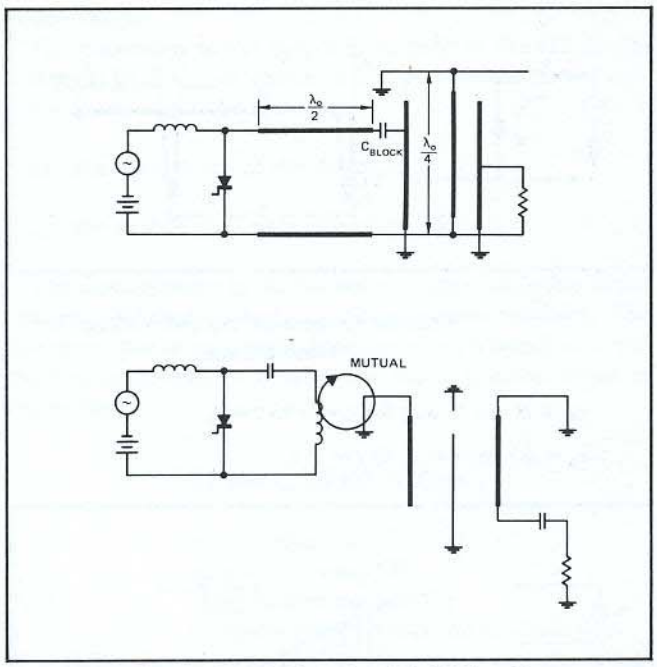


Figure 8. Examples of Complete Multiplier Prototypes

Summary of Design Procedure

Figure 10 shows a summarization of the design procedure of an SRD multiplier. At each step of the way it is possible to check the behavior in a 50 Ω system. This is an important factor in practical design procedures. In the next section each step of the design is considered in more detail.

Assumptions:

a) $Z_o > \sqrt{L/C_{VR}}$

b) $1/2f_o < t_p > 1/f_o$

c) Transition time small compared to desired pulse width

d) Quasi voltage generator realizable

e) Diode: two state device

Assumptions:

a) $Q_\ell \approx (\pi/2)n$

b) bw required $< \dfrac{f_o}{(\pi/2)n}$

a) $bw << f_o/n$

(filter 3dB bw less than $\dfrac{f_o}{(\pi/2)n}$)

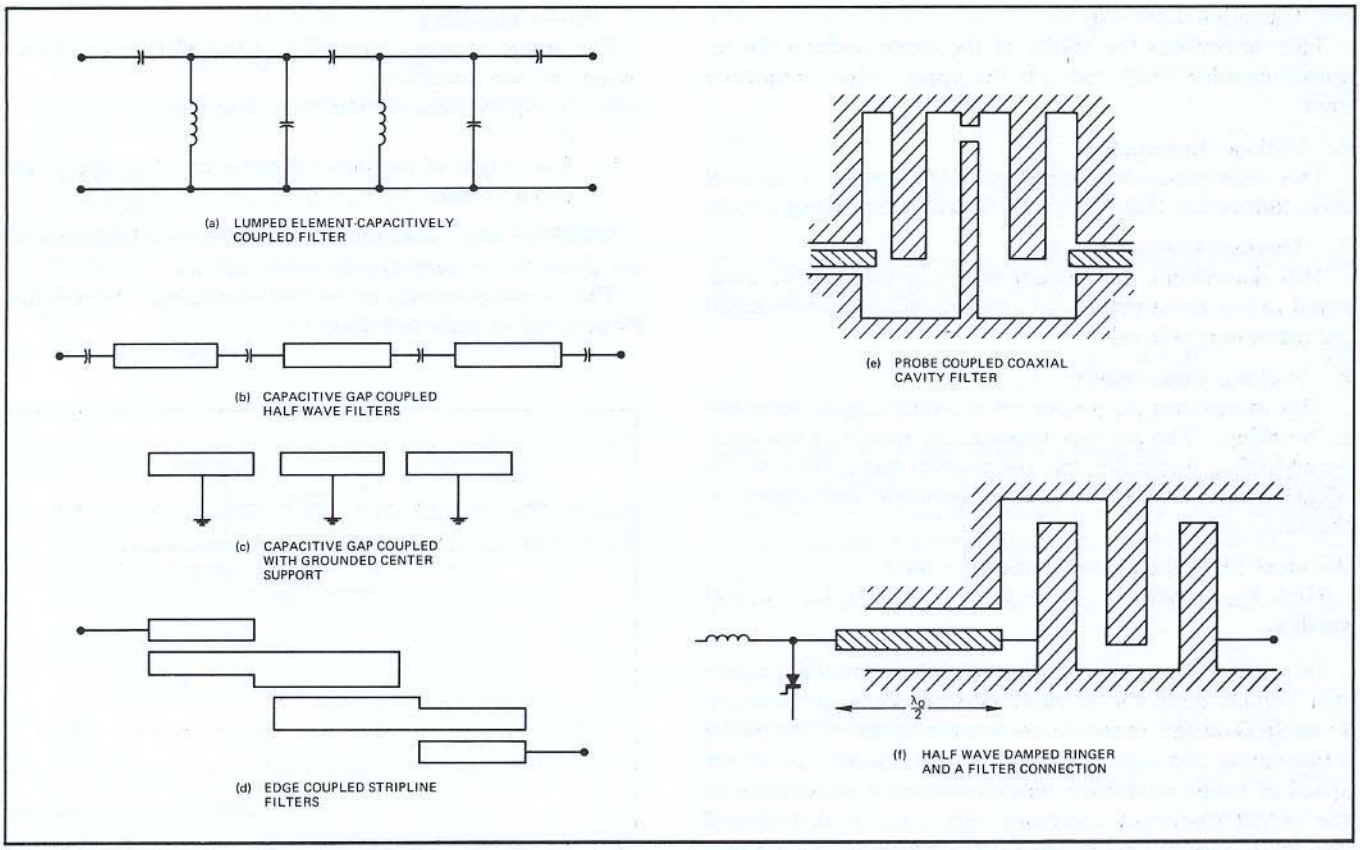


Figure 9. Multiplier Output Filter Circuits

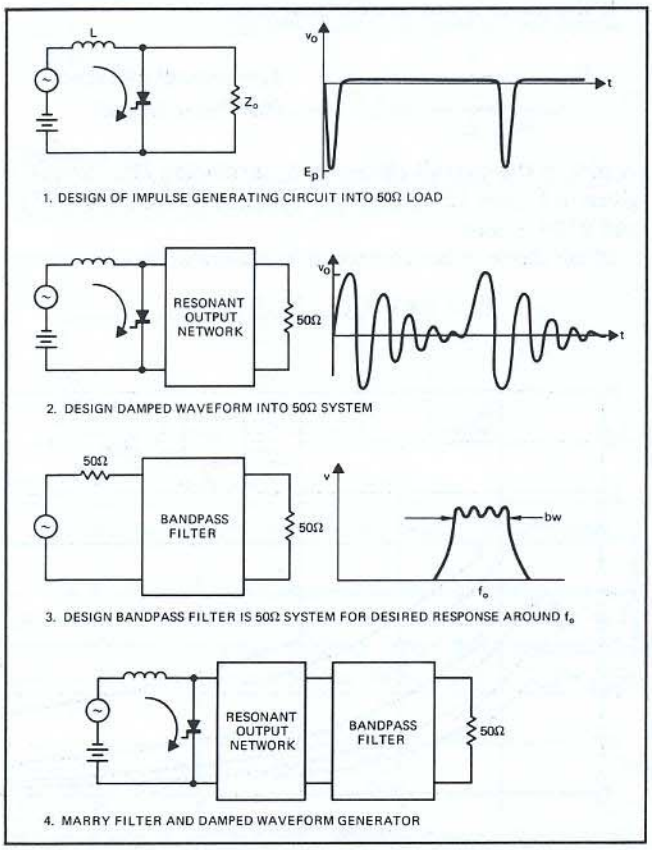


Figure 10. Summary of SRD Multiplier Design

Multiplier Design Procedure

Before a multiplier can be designed, certain system requirements must be known. These are: output frequency, output power, input frequency and bandwidth. Based on these, the design proceeds in the following sequence: diode selection, design of the impulse generator, design of resonant line circuit, and design of output filter.

a) Diode Selection: The important parameters of the SRD as far as the design of an impulse generator is concerned, are:

1. Breakdown Voltage: V_{BR}

This determines the maximum amplitude of the impulse and the energy in the impulse $U_c = 1/2\, C_{VR}\, E_p^2$

2. Reverse Bias Capacitance: C_{VR}

In addition to determining the energy in the impulse, C_{VR} also determines the impedance level of the ringing line. This capacitance is specified at -10 volts bias, since even the highest breakdown voltage SRD exhibit punch-through capacitance at this bias.

3. Series Resistance: R_S

This determines the loss that will occur in the ringing line and in the diode input circuit.

4. Minority Carrier Lifetime: τ

This determines the loss that occurs during forward charge storage due to carrier recombination as well as the value of the bias resistance, which develops the diode bias due to rectification current.

5. Transition Time: t_t

This determines the ability of the diode to form the required impulse width and sets the upper output frequency limit.

6. Package Inductance: L_p

This determines the proportion of the energy in the total drive inductance that is not transferred to the ringing circuit.

7. Thermal Resistance: θ_{jc}

This determines the amount of power that can be dissipated in the diode before the junction temperature reached the maximum safe value.

8. Package Capacitance: C_p

This determines the proportion of overall capacitance that is "working." The package capacitance should be low compared to C_{VR}. Typically, this condition is met more easily in SRD's than in varactors because junction capacitance is higher.

An ideal SRD should simultaneously have:

High V_{BR}, small C_{VR}, $R_S = 0$, $\tau = \infty$, $t_t = 0$, $L_p = 0$, and small θ_{jc}.

In practice, materials and fabrication techniques require that certain tradeoffs be made between these parameters. In an SRD design, these parameters are traded off to achieve a fast-acting two-state storage device of low loss. Since the speed of action (transition time) increases in importance as the output frequency increases, this suggests that several designs of diodes are required, each covering its own segment of a broad frequency range. Each diode within the series is then optimized for the best tradeoff of parameters in its own frequency range. Although any varactor, or for that matter, any *pn* junction, will exhibit all of the above parameters, it will not usually have these properly optimized for step recovery action and the critical parameters are not necessarily sufficiently well controlled. A list of available HP SRD's is given in Table I. Some of the tradeoffs that have been made are evident in this table.

Diode Selection

We assume the diode to be used is the Shunt Mode described in this note. The diode is first selected from Table I by calling out the output frequency. The four basic diodes cover S, C, X, and Ku bands respectively; the diode reactance (at band center) and the transition times are appropriate to each of the bands. These are based on the following rules of thumb:

1. Transition Time $t_t \leq 1/f_o$

2. Impedance Level $10 < X_o < 20\Omega$ (approximate, assumes 50 Ω system)

   where $X_o = \dfrac{1}{2\pi f_o C_{VR}}$

3. Lifetime $\tau >> \dfrac{1}{2\pi f_{in}}$ ($\omega\tau > 10$ is adequate for most purposes)

4. Package Inductance $L_p < \dfrac{X_o}{\omega_o}$

5. Power Handling

The power handling capability of the SRD is controlled by one of two limitations:

a) The power dissipation exceeding $P_{diss\ max}$, or

b) The height of the impulse exceeding V_{BR}, the breakdown voltage.

Which of these is the limitation (if there is a limitation for the given power output) is found as follows:

The overall efficiency of the SRD multiplier is broken into its descriptive parts in Figure 11.

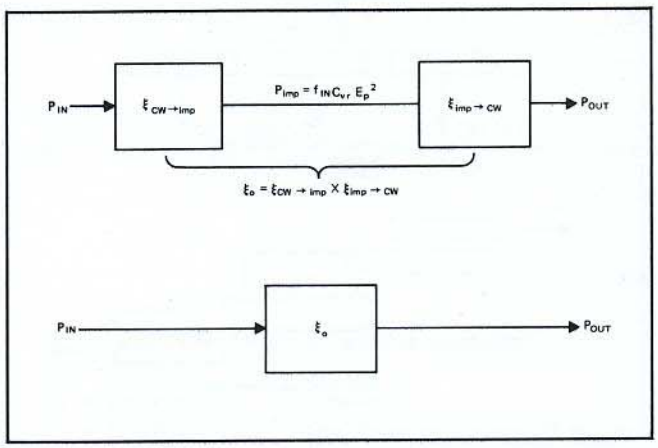


Figure 11. Efficiency Diagram

If the diode is not to overheat, then:

$$P_o < \frac{1}{\dfrac{1}{0.63\ \xi_o} - 1} P_{diss_{max}}$$

ξ_o = overall efficiency [See Note below]

A plot of the overall efficiency ξ_o (excluding filter losses) is given in Figure 12 for $n = 5$, 10, 15, and 20, and 0300, 0310, and 0320 diodes.

If the diode is not to exceed breakdown, then

$$P_o < 0.63\ (f_i\ C_{VR}\ V_{BR}^2)\ \xi_{imp \rightarrow CW}$$

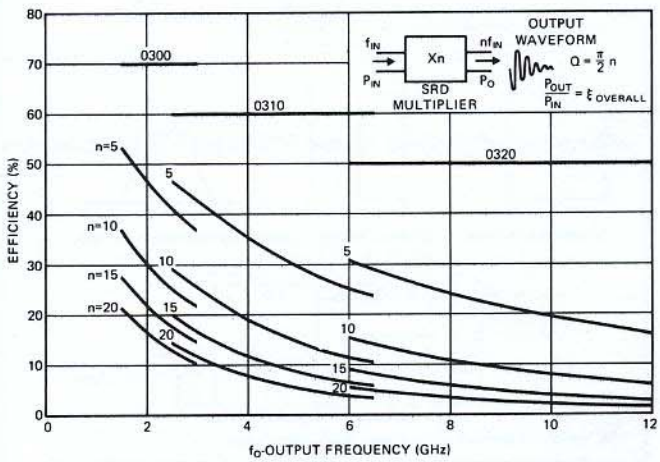


Figure 12. Overall Efficiency

Table I—SRD Characteristics

	0300	0360	0365	0310	0370	0320	0375	0330	0380
Output Freq. Range (GHz)	1.5-3.0	1.5-3.0		3-7	3-7	5-12	5-12	12-18	12-18
Test Frequency (GHz)	2			6		10		16	
Power Output Range (watts)									
n = 5	4.5-2.75			1.2-1		0.6-0.4			
n = 10	2.45-1.45			0.5-0.4		0.2-0.150			
Min. Test Spec (watts)	2 (×10)			0.4 (×10)		0.150 (×5)			
Input Test Freq. (GHz)	0.400			0.6		2		2	
Power Input Range (watts)	0.2-15	0.2-15	0.2-10	0.2-7	0.2-7	0.2-4	0.2-4	0.2-2	0.2-2
Spec (watts)	10			4		2		1.5	
Achievable Pulsewidths (ps)	150-750	150-750	125-500	100-325	100-325	75-125	75-125	50-100	50-100
P_{diss} (max) (watts)	9	9	7	6	6	3.6	3.6	1.5	1.5
Package Inductance (nh) (Microstrip configuration)	0.3	0.3	0.4	0.3	0.3	0.3	0.3	0.1	0.1
V_{BR} (volts)	75	80-110	50-85	40	40-60	20	25-40	18	18-28
C_{VR} (including package capacitance) pF	2.5-6.5	3.5-6.5	2.5-4.1	1.9-3.5	1.9-3.1	0.65-1.3	0.8-1.6	0.8-1.3	0.8-1.3
R_S (ohms)	0.12	0.12	0.3	0.4	0.4	0.8	0.8	1.0	1.0
τ (nanoseconds)	>100	150-400	80-240	>50	50-150	>10	20-60	>20	20-60
t_t (picoseconds)		<650	<300		<200		<120		<120
Θ (°C/watt)	20	20	25	30	30	50	50	110	110
Max. Junction Temperature (°C)	200	200	200	200	200	200	200	175	175

The impulse to CW efficiency for each of the diodes is shown in Figure 13. This together with the input frequency, diode capacitance and the above equation will show whether breakdown voltage is a limitation. If both of the equations are satisfied, there is no diode power handling problem and the design of the multiplier may begin.

Note: The factor of 0.63 in these equations is a good estimate for the conversion of the damped waveform to pure CW at nf_i. It includes 0.8 dB filter loss. The assumption that $Q = \pi/2n$ means that 76% of the total damped waveform power is in the nth line. The 0.63 combines these two effects.

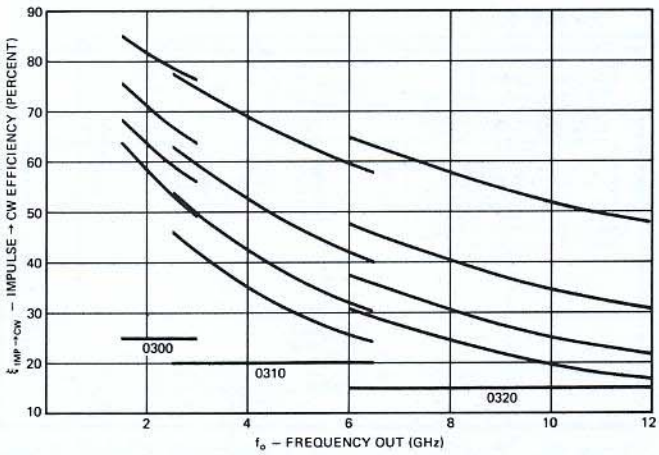


Figure 13. Efficiency of Converting the Impulse to a Damped Waveform, $\xi_{imp \rightarrow cw}$

Figure 14 shows the derating for HP diodes whose maximum junction temperatures are 175°C and 200°C. The maximum junction temperatures for various "use tested" and midline diodes are shown in Table I.

——— Derating for diodes having $T_{j_{max}} = 200°C$. (See Table I.)

. . . . . Derating for diodes having $T_{j_{max}} = 175°C$. (See Table I.)

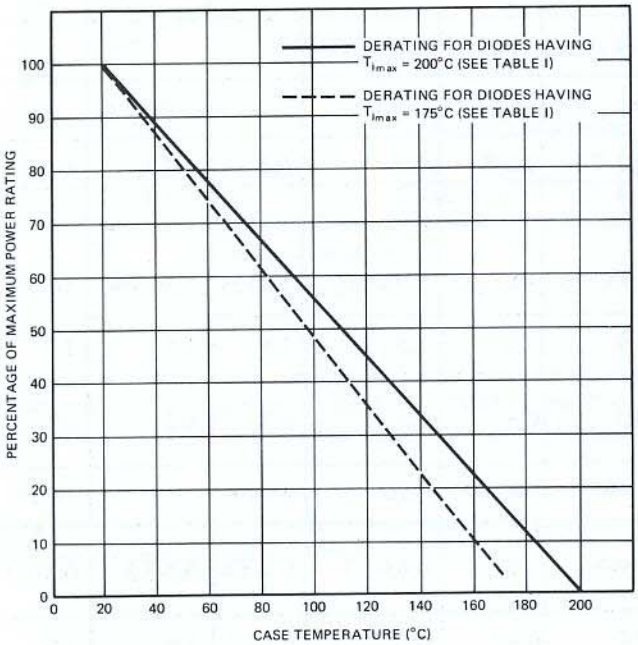


Figure 14. Maximum Power Derating Curves

b) Design of the Impulse Generator: Figure 15 shows a practical realization of the impulse generator. The circuit consists of:

1. The appropriate step recovery diode.
2. A driving inductance, L and an RF capacitor, C_T, to tune it out at f_i.
3. A matching network from 50 Ω to R_{in} of the circuit.
4. A bias network, which can alternately be used to introduce DC bias or to provide connection to a bias resistor for self bias.

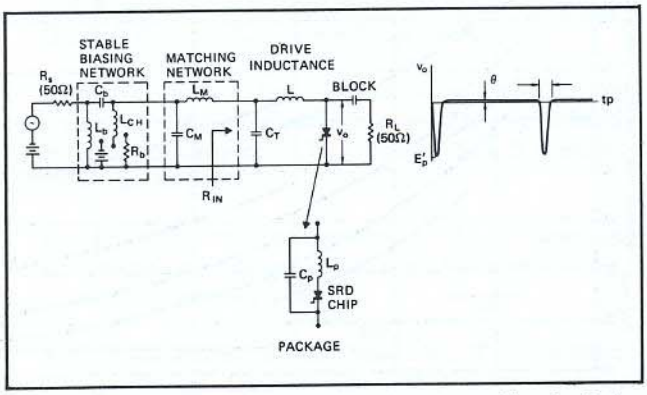


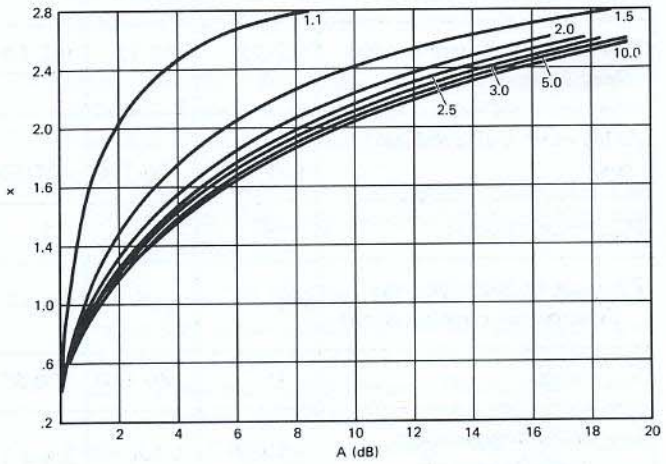
Figure 15. Practical Impulse Generating Circuit Using Step Recovery Diode. The voltage across R_L is a negative half sine pulse once per cycle, of width $\pi\sqrt{LC_{VR}}$ seconds.

Required Pulse Widths

This specific circuit has two important uses: 1. As a "comb" generator. 2. As the key element in a CW multiplier.

1. Comb Applications

For the comb generator, the pulse width, t_p, is chosen based on where the first zero in the line spectrum is to occur, ($f = 3/2\ t_p$), or on the power variation required between two harmonics of f_i. From the curve and expressions in Figure 4 it is clear that the pulse width, t_p, will determine the power variation between two harmonics of f_i, say n_1 and n_2. Figure 16 permits the determination of the required pulse width for comb applications.



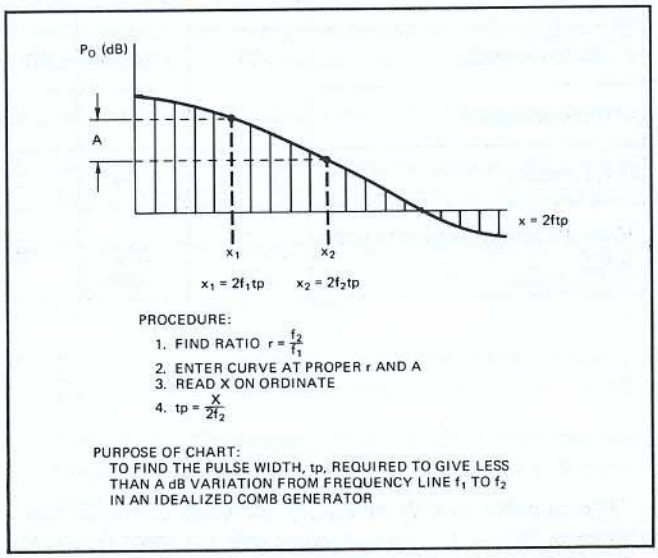


Figure 16. Pulse Widths for Flatness of Comb from n_1 to n_2

2. Frequency Multipliers

For CW frequency multipliers, the pulse width should be approximately a half cycle at the output frequency (e.g., Ref. 1). Experiments have shown however, that it is **not** necessary that the pulse be **exactly** $1/2\ f_o$. In fact, overall efficiency benefits from slightly wider pulses because they can be generated so much more efficiently. The optimum pulse width, as shown in the efficiency curves in the Appen-

dix, is generally greater than $1/2\, f_o$ but less than $1/f_o$. Consequently, for CW multipliers, the design pulse width for the impulse generator is in the range:

$$\frac{1}{2f_o} < t_p < \frac{1}{f_o}$$

Element Values; Impulse Generator

The damping factor, ζ, of the circuit, is best set at 0.3, for good power output and pulse shape.

$$\zeta = \frac{1}{2R_L}\sqrt{\frac{1}{C_{VR}}} = \frac{t_p}{2\pi R_L C_{VR}} \qquad \text{(Should be } \zeta \approx 0.3\text{)}$$

The drive inductance is calculated (at first assuming the transition time, t_t, of the diode is zero) from:

$$L \cong \left(\frac{t_p}{\pi}\right)^2 \frac{1}{C_{VR}}$$

Ideally, this L would give an impulse of width t_p. Non-zero t_t widens the pulse by:

$$t_p'' = t_p\sqrt{1 + \frac{t_t^2}{t_p^2}} \qquad \text{negligible for } t_t < 1/2\ t_p$$

L may need to be lowered accordingly.

The tuning capacitor, C_T, resonates out L at f_i. Its value is approximately:

$$C_T \cong \frac{C_{VR}}{(2f_{in}t_p)^2}$$

This capacitor carries the RF current at all n harmonics of f_{in} (up to $f = 3/2\ t_o$); it must be a good RF capacitor. Its physical dimensions must be less than $\lambda/4$ at $f = 1/(2\ t_p)$*. At high frequencies, this may require Thin Film or MOS capacitors.

Matching Network

The matching network of Figure 15 is a two-element network, adequate in bandwidth for most applications. The input impedance at terminals of C_T is a pure resistance, R_{in}; where (see Ref. 1):

$$R_{in} \simeq \omega_i L \text{ and } \omega_i = 2\pi f_i$$

When $R_g/R_{in} > 10$, then the values for the matching components can be obtained from (see Ref. 16):

$$L_M = \frac{X_M}{\omega_i} \cong \frac{\sqrt{R_g R_{in}}}{\omega_i}$$

$$C_M = \frac{1}{X_M \omega_i} \cong \frac{1}{\sqrt{R_g R_{in}}\,\omega_i}$$

These matching elements provide an input bandwidth of

$$BW \cong \frac{2f_{in}}{\sqrt{\frac{R_g}{R_{in}} + 1}} \qquad (BW \text{ to } P_{refl} = 1/2\ P_{in}) \text{ point}$$

Broader bandwidth matching sections are described in Ref. 17.

Resonant Output Network

The next step in CW multiplier design is to resonate the output of the impulse generator at f_o. One of the resonant networks of Figure 6 is used for this. Consider now, in detail, the $\lambda_o/4$ type resonator, Figure 6a.

$$Q \cong \pi/4\left(\frac{X_c}{Z_0}\right)^2 = (\pi/2)n$$

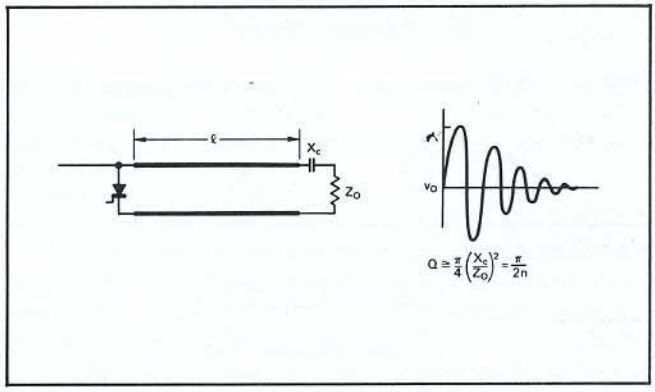


Figure 17. Resonant Output Network

The Q shown should be set $\cong (\pi/2)n$ for good operation. The coupling capacitance can then be found to be

$$X_c \simeq \sqrt{2n}\ Z_o = 1/\left(2\ \pi f_o C_c\right) \qquad C_c = \frac{1}{\omega_o Z_o \sqrt{2n}}$$

Because the line is terminated reactively and resistively, ℓ will be shorter than $\lambda_o/4$. This is normal for resonant lines with capacitive end loading. The foreshortening, $\Delta\ell$, may be estimated by (Ref. 18, p. 437):

$$\Delta\ell = \frac{\lambda_0}{2\pi}\tan^{-1}\frac{1}{\sqrt{2n}}$$

where the total length required in Figure 2 is

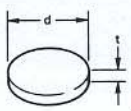
$$\ell \simeq \frac{\lambda_o}{4} - \Delta\ell$$

Similar expressions may be developed for the other coupling networks shown.

For good impulse formation, Z_o must not overload the impulse generator; this is true if:

$$Z_o > \sqrt{\frac{L}{C_{VR}}}$$

*The electrical diameter of a round parallel plate capacitor depends only on the spacing of the plate (not ϵ_r).



$$C = \frac{\pi\epsilon_r\epsilon_0 d^2}{4t}\ ;\ d_{electrical} = \sqrt{\epsilon_r}\, d$$

$$\therefore C = \frac{\pi}{4t}\,\epsilon_0 d^2_{elect.};\ \text{(independent of } \epsilon_r\text{)}$$

Therefore, the only way to make a capacitor smaller is to make it thinner.

Final Filtering

Many types of output filters have been used in conjunction with the SRD to form a multiplier. (See Figures 8 and 9.) Consider Figure 9b as an example of final filtering in an overall multiplier.

For narrowband (lightly loaded) case, the required coupling capacitor in such a filter may be estimated by symmetry:

$$Q = \frac{f_o}{\Delta f} = \frac{\pi}{4}\left(\frac{R_{eff}}{Z_o}\right) = \frac{\pi}{4}\left(\frac{X_c}{Z_o}\right)^2$$

Δf = bandwidth f_o = center frequency

$$\therefore \frac{\Delta f}{f_o} = \frac{4}{\pi}\left(\frac{Z_o}{X_c}\right)^2$$

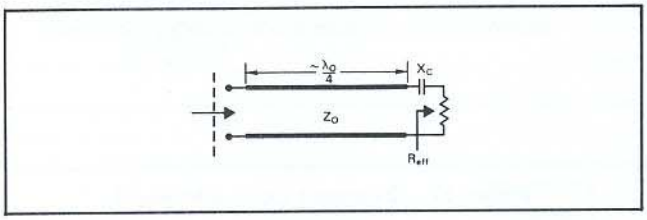


Figure 18

The bandwidth of an Xn multiplier is limited, fundamentally, by the requirement that no more than one line appear at the output simultaneously. Figure 19 shows the fundamental limit on the bandwidth, assuming that the input is swept from f_{iL} to f_{in}. The limiting bandwidth is

$$\Delta f \leq \frac{f_{oL}}{n} = f_{iL}$$

For practical filters, where non-infinite Q's are involved, this limit should be reduced to $f_{iL}/2$. Using this relationship, the coupling capacitance may be found for the maximum bandwidth case to be:

$$\frac{\Delta f}{f_o} \simeq \frac{1}{2n} = \frac{4}{\pi}\left(\frac{Z_o}{X_c}\right)^2$$

$$\therefore C_c = \frac{1}{\omega_0 Z_0}\sqrt{\frac{\pi/4}{2n}}$$

Hence, the coupling capacitance for the filter, and the damped waveforming network are nearly the same in this particular case. The added attenuation of the $(n-1)$ and $(n+1)$ sidebands for this one element filter would be about 12 dB (total of about 17 dB down from nf_{in}). Additional elements (with maximally flat design) would add about 12 dB per element at maximum bandwidth operation of $1/2n\%$.

An alternate method of design of the output network is to view the diode as a voltage generator of the impulse with an internal resistance equal to R_S, the series resistance of the diode. A filter design (Ref. 18, Section 11.08) may be evolved directly. One constraint must be added, however, so that the impulse formation is not disturbed – the transient impedance must be greater than $\sqrt{L/C_{VR}}$.

$$Z_{transient} > \sqrt{L/C_{VR}}$$

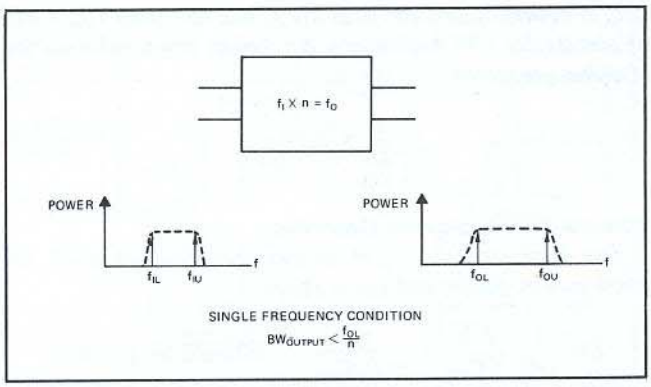


Figure 19. Bandwidth Limitations in Multipliers

Biasing

While the SRD has little rectification current, still a small amount ($\Delta q \approx 1/2\, f_{in}\tau$) of charge does recombine per cycle (τ = lifetime). The dc current flow follows $i_{dc} = q_0/\tau$, where q_0 is the total stored charge.

$$q_o \cong \frac{2I_p}{\omega_i}$$

$$\therefore i_{dc} \cong \frac{2I_p}{\omega_i \tau}$$

This dc rectified current approaches zero as $\tau \rightarrow \infty$. The bias required for the SRD may be developed by i_{dc} through R_b as shown below.

$$E_p \cong \pi N (V + \phi) \therefore R_b \simeq \frac{2\tau}{\pi C_T N^2}$$

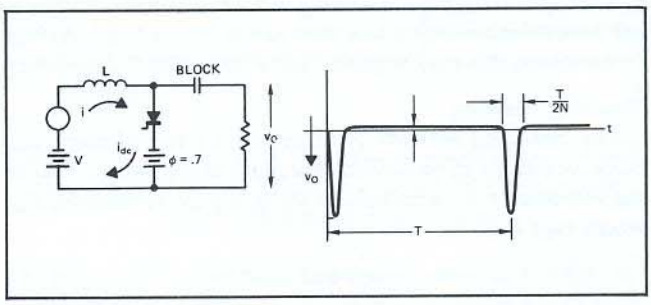


Figure 20. Self Bias Relationships, SRD Impulse Generator Circuit

The Bias Network

While conventional, commercially available bias tees may be used for bringing dc to the diode (whether self or external bias is used), the specific problems of stability in SRD frequency multipliers should be considered in the selection of a bias tee. In Section V, the stability of SRD multipliers is related to the impedance seen by the diode below f_i. Specifically, no high Q series resonances should be allowed, especially at low frequencies.

The bias arrangement, shown in Figure 15, meets these requirements when the choke, L_{CH}, is not bypassed to ground and when no self resonances (of the series type) occur in any of the elements.

The values of L_b and C_b are chosen to form a high pass filter with $f_{co} \cong 0.8\, f_i$. For a maximally flat high pass filter this becomes

$$L_b = \frac{24.4}{f_i\,(GHz)} \text{ nanohenries}$$

$$C_b = \frac{8.85}{f_i\,(GHz)} \text{ picofarads}$$

This network **must** be located close to the diode, electrically closer than $\lambda_i/4$ at the input frequency. This is due to the fact that a high pass filter, below cutoff, appears as an open; and transformed $\lambda_o/4$, this would again be a short across the diode at some $f < f_{in}$.

III. Multiplier Design Examples

In this section we will give detailed multiplier design examples using step recovery diodes in standard packages. Several examples will be given, covering the UHF, S, C, and X bands. Three designs will be described in S band; one, a times 5, broadband unit with a power output of 2.5 watts; another, a times 5, narrow band unit with higher power; and the third, a times 10.

The reason for the variety of examples is to illustrate different techniques that are useful when one progresses from relatively low frequencies of $\approx$ 60 megahertz to the very high frequencies of thousands of megahertz.

At low frequencies, conventional RF inductors, capacitors, and resistors can be used. Likewise, measurements of different waveforms throughout the circuit can be made accurately and with a minimum of effect on circuit operation. In general, the function of each circuit element and its interaction with the others can be readily determined and understood, as will be shown in the case of the UHF multiplier design. This is not the case at higher frequencies. As the frequency increases, it becomes increasingly more difficult to realize "lumped" circuit elements, and to identify and control their contribution. This applies to the diode and its parasitic elements, as well as to the measuring probes, to the extent that their presence modifies the circuit conditions. In such cases, the final design is highly empirical. This is the case of the X-band multiplier design. Although largely empirical in realization, it does illustrate that good high frequency switching reactance multipliers using packaged diodes are possible although point-by-point explanations of their operation are not.

These difficulties are, in fact, what led us to the hybrid integrated designs described in Section IV. Here, much of the designer's time that would normally be used in laboratory optimization has been eliminated by the availability of a complete input circuit.

Design Example 1

This example illustrates the design of a practical impulse train generator and the resonant output circuit forming the damped waveform. Low frequency is used to illustrate the application of theory and to render all critical waveforms measurable with standard equipment. The input frequency is 60 MHz and an output frequency is 300 MHz.

Diode Choice

The low output frequency (at 50 Ω level) requires the use of a large capacitance diode or several diodes in parallel. For a reasonable diode reactance of 10-20 Ω the required C_{VR} is

$$C_{VR} = \frac{159}{13\ (10-20)} = 53\text{-}26 \text{ pF}$$

This can be satisfied by four 8-9 pF diodes in parallel. Total $C_{VR} \simeq 36$ pF. A suitable diode would be an HP 0133.

Impulse Generator

The circuit of the desired impulse generator is shown in Figure 21a.

(a) Impulse Generator

(b) Impulse Generator Plus Resonant Output Network

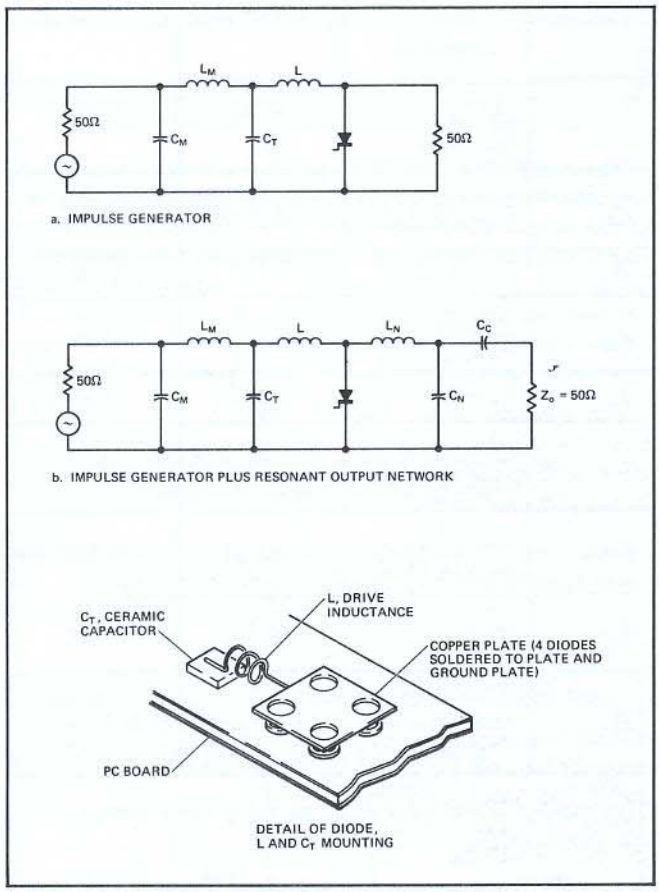


Figure 21. Configuration Used in n=5, 60 MHz to 300 MHz Multiplier

Notes on Construction

1. 4 diodes [$C_{-10} = 8$ pF] were paralleled; common plate used to keep diodes at same temperature and potential.

2. Capacitors used were cut from commercial ceramic (metallized) disks: such as American Lava ALSIMAG T-157A (K ≅ 275).

3. Coils wound using standard coil formulas; for example, ITT Federal Handbook, Fourth Edition "Reference Data for Radio Engineers," pg. 112.
4. Circuit built on copper-clad P.C. board.

For illustration purpose, let us design two impulse generators (using circuit of Figure 21a) one with a half-cycle pulse width, and the other with a one-cycle pulse width (at f_0=300). For 300 MHz output, t_p is

$$t_{p1} = \frac{1}{2f_o} = 1.67 \text{ nsec}$$

$$t_{p2} = \frac{1}{f_o} = 3.34 \text{ nsec}$$

The values of the circuit components are then:

Table II – Element Values; UHF Example $C_{VR} \cong 35\ pF$

Circuit Element	Equation	$t_{p1} = 1.67$ *nsec*	$t_{p2} = 3.34$ nsec
L	$\left(\frac{t_p}{\pi}\right)^2 \frac{1}{C_{VR}}$	8 nh	32 nh
C_T	$C_{VR}/\ (2f_i\ t_p)^2$	865 pF	216 pF
R_{in}	$\approx \omega L$	3 Ω	12 Ω
L_M	$\frac{\sqrt{R_g R_{in}}}{2\pi f_{in}}$	32.5 nh	65 nh
L_N	$L_N = L$	8.0 nh	32 nh
C_M	$\frac{1}{2\pi f_{in}\sqrt{R_g R_{in}}}$	216	108 pF
C_C	$\frac{1}{\omega_o \sqrt{\omega_o L Q Z_o}}$	8.7 pF	2.16
C_N	$\frac{1}{\omega_o{}^2 L} - C_C$	26.3 pF	6.6 *pF*
Q	(Optimum experimentally determined)	$Q \approx n=5$	$Q \cong 4n = 20$

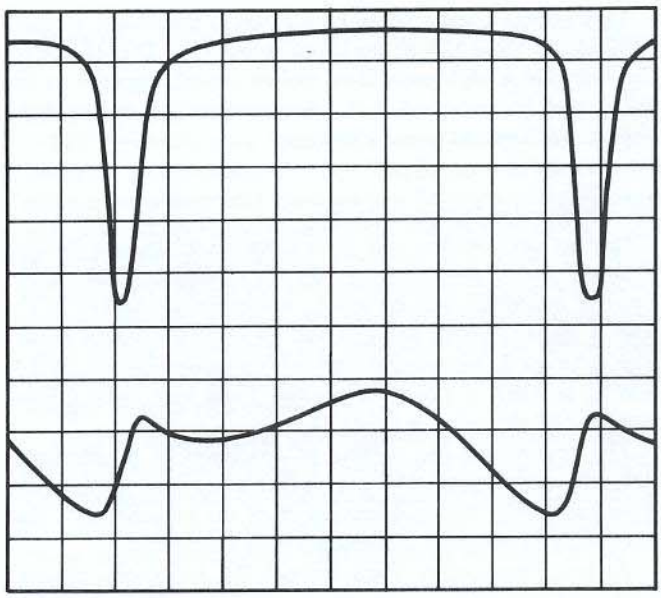
The impulse waveforms obtained using these circuit values are shown in Figure 22, a and b.

Characteristics of Impulse Train

	$t_p = 1/f_o$	$t_p = 1/2\ f_o$
Power Input	3 W	1 W
Power Reflected	0.1 W	0.3 W
Power Output	2.1 W	0.532 W
Efficiency	72.5 %	75.0%
Bias	3.8 V	2 V

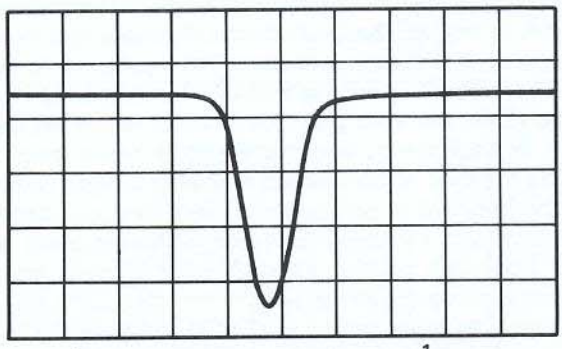
a) Waveform for $t_p = 1/2f_o$
$V = 2$ V/cm
$I = 0.5$ A/cm
$t = 2$ nsec/cm

b) Waveform for $t_p = 1/f_o$
$V = 10$ V/cm
$t = 2$ nsec/cm



(a) WAVEFORM FOR $t_P = \frac{1}{2f_O}$

V = 2V/cm
I = .5A/cm
t = 2 nsec/cm



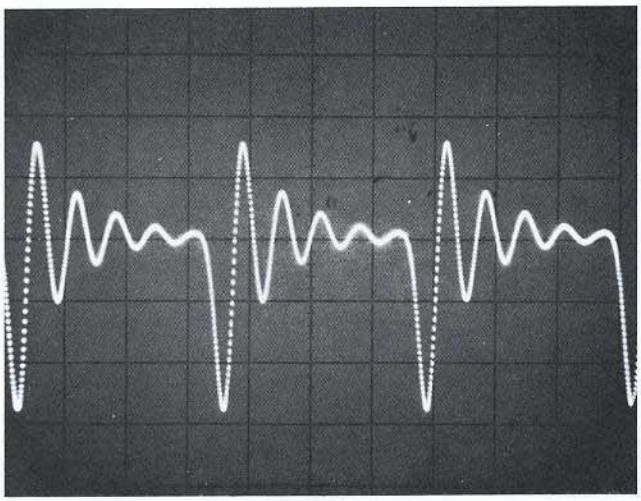
(b) WAVEFORM FOR $t_P = \frac{1}{f_O}$

V = 10V/cm
I = .5A/cm
t = 2 nsec/cm

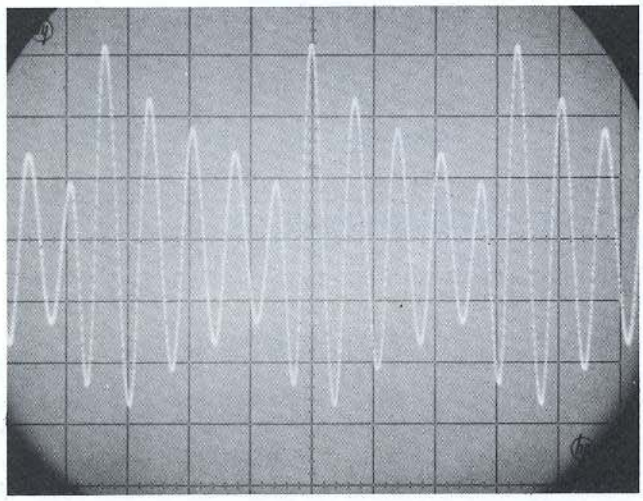
Figure 22. Impulse Waveforms for 300 MHz Example

Shown are the diode voltages across the 50 Ω load resistor. The current flowing in the diode is also shown for the $t_p = 1.67$ nanoseconds case (a). The current was monitored by measuring the voltage across a 0.1 Ω resistor chip under the diodes.

Damped Waveform: The lumped element resonant output circuit of Figure 6c was used in the formation of the damped ringing waveform in each of these two cases. In each case, maximum output was obtained when $L_N \equiv L$, with C_C and C_N being adjusted to resonate the network and adjust the loading (Q_l). The two resulting waveforms are shown in Figure 23, a and b.



a) Damped Waveform for $t_p = 1/2f_o$
Scale: Vertical: 10 V/cm
Horizontal: 5 nsec/cm



b) Damped Waveform for $t_p = 1/f_o$
Scale: Vertical: 5 V/cm
Horizontal: 5 nsec/cm

Figure 23. Damped Waveforms

Characteristics of Damped Waveform Generator

	$t_p = 1/2f_o$	$t_p = 1/f_o$
Power Input	3 W	2 W
Power Reflected	0.26 W	0.14 W
Power Output	1.6 W	1.05 W
Efficiency	58.5 %	56.5 %
Bias	1.2 V	3.9 V
Q_L	$\approx n$	$\approx 4n$

It is seen that even though the pulse width is not exactly a half cycle at the output frequency (at the impulse generator design stage) the Q_l of the output network can be increased to bring the output power level up. This of course is done at the sacrifice of bandwidth in the t_p=$1/f_0$ case; the t_p=$1/2f_0$ case is more consistent with the wideband requirements however (since the required Q_l is lower).

Because the Q_l of the output circuit for the $t_p = 1/f_o$ case was required to be much higher, there was considerable energy left in the input circuit at the end of each cycle. This caused a change in input impedance from about 12 Ω to 3 Ω. Accordingly, the values of C_M and L_M were changed from

$$L_M = 65\ nh \text{ to } 32\ nh$$
$$C_M = 108\ pF \text{ to } 216\ pF$$

The circuit element values called out in Table II, for this X5, 60 to 300 MHz multiplier may be scaled for other X5 multipliers operating at different output frequencies. In practice, multipliers scaled to 2 GHz and to 10 GHz have been built quite successfully. The 2 GHz scaled unit will be described in a later example.

Design Example 2: A X5 and a X10 S-Band Multiplier

Requirements:

X5	X10
f_{in} = 400	200
f_0 = 2000 MHz	2000
P_o = 4 watts	2 watts

Diode Selection

For high power CW multiplier applications in the f_0 = 1.5 to 3 GHz range, we recommend the HP 0300 SRD. This diode has adequate power handling capability, and has been designed to provide pulses of width appropriate to this frequency range. The C_{VR} capacitance of the 0300 is: $C_{VR} \cong 4\ pF$. The lifetime of the 0300 is sufficiently large and the diode can be used for the low frequency input design.

Impulse Generator Designs

For $f_0 = 2$ GHz; 250 ps $< t_p <$ 500 ps
choose $t_p = 350$ psec; $C_{VR} = 4$ pF

The Impulse Generator prototype circuit is the same as in Figures 15 and 21a. The element values are calculated as in Table II. The element values are given in Table III.

Table III – Element Values, *S*-Band Impulse Generators

Element	$f_{in} = 400$ MHz X5	$f_{in} = 200$ MHz X10
L	3.1 nh	3.1 nh
C_T	50.6 pF	200 pF
R_{IN}	7.8 Ω	3.9 Ω
L_M	7.85 nh	11.1 nh
C_M	20 pF	59.4 pF

Resonant Output Network

For this application, a transmission line λ/4 long at 2 GHz (Figure 6a) was used. The required impedance of this line is the same for both multipliers

$$Z_o > \sqrt{L/C_{VR}}\,;\; Z_o > 28\ \Omega$$

($Z_0 \approx 35\ \Omega$ actually used)

the required Q_l of the loaded line is

	X5	X10
$Q_l = \pi/2\ n$	7.5	15
$R_{eff} = 2nZ_o$	≈ 350 Ω	≈ 700 Ω

In order to test the damped waveform generator before coupling it to the filter, the resonant line can be coupled to a 50 Ω load via an air gap coupling capacitor in the center conductor of the line. The required value of this coupling capacitor is

$$C_C = \frac{1}{\sqrt{2n}}\left(\frac{1}{\omega_o Z_o}\right)$$

It is, however, usually simpler to adjust the gap in the center conductor using a fixture such as shown in Figure 24.

Final Filtering Design

A bandpass filter was first built and tested in a 50 Ω system. It was an *E* field probe-coupled, 2-element, coaxial, quarter-wave resonator filter. The insertion loss was about 1 dB, with a bandwidth of 15 MHz at 2000 MHz. The final multiplier was formed by replacing the input probe of the filter with the λ/4 wave resonant output line and the impulse

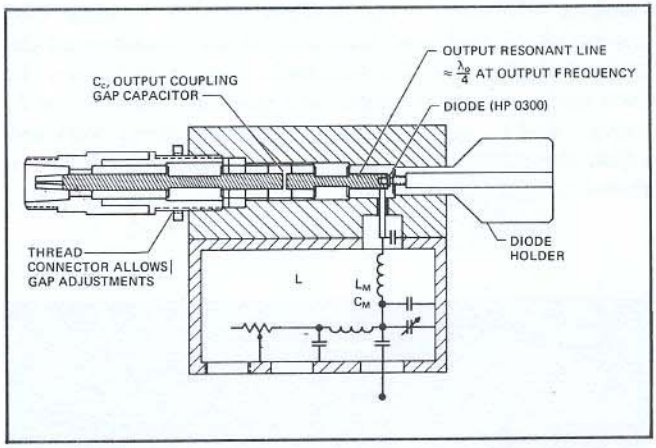


Figure 24. Damped Waveform Test Fixture

generator. Minor adjustments* of the depth of this probe were used to optimize the power output.

A cut-away view of the final S-Band Multiplier (same basic design was used for both units) is shown in Figure 25, and the power outputs obtained are shown in Figure 26.

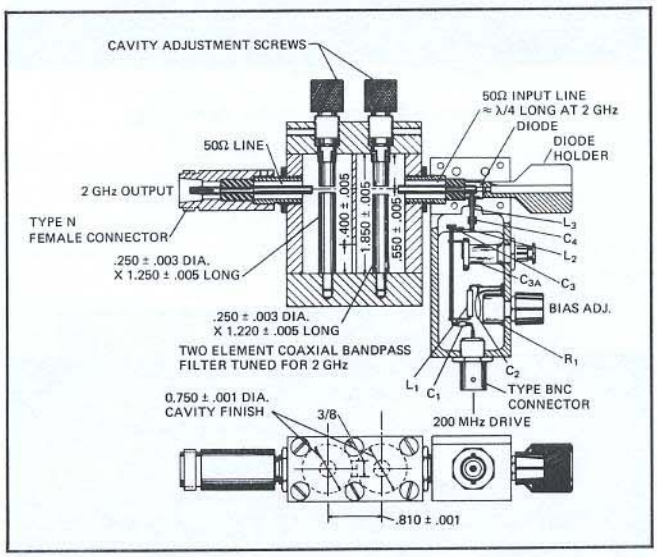


Figure 25. Mechanical and Electrical Layout of an S-Band Harmonic Multiplier (X5 and X10, same layout)

Design Example 3. S-Band Multiplier

This is an example of a 2 GHz multiplier which was scaled from the 60 → 300 MHz multiplier design. The objective here was to establish a broader bandwidth capability than that achieved in previous designs. The bandwidth of any multiplier is theoretically limited to ~ $1/n\%$, as was seen in Figure 19. In practice, another factor of 2 enters in because of finite Q's of the output filters.

* In steps as small as 0.005". First cut was the depth of the 50 Ω filter probe. This was very close. The desired coupling capacitance may be estimated as was outlined in the previous section. (Figures 17 and 18.) The probe depth may then be found from available data (Moreno, Ref. 19, p. 102).

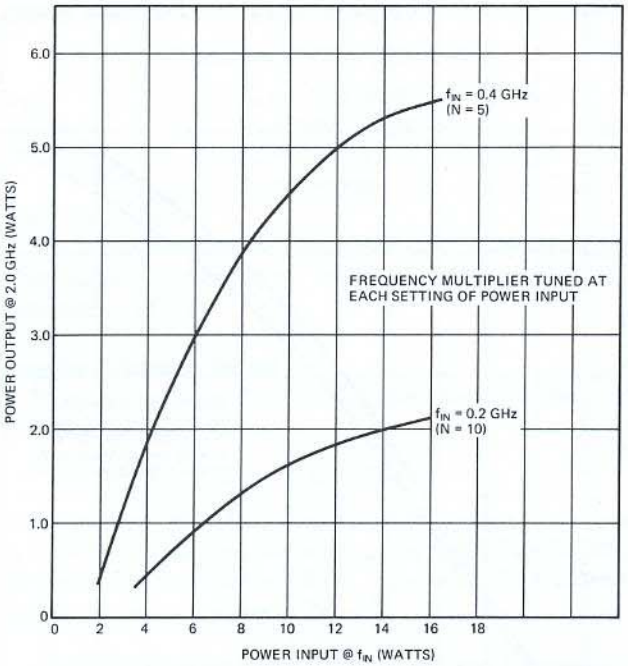


Figure 26. Power Output, S-Band Multipliers (X5 and X10 to 2 GHz)

Multiplier Design Objectives

f_i = 400 MHz

f_o = 2000 MHz

BW = maximum possible consistent with good overall performance

In this design, a lumped element output resonator (Figure 6c) was used instead of a $\lambda_o/4$ wave line. The 0300 diode was used again in this circuit.

The network used is shown in Figure 21b. The scaled parameter values from the low frequency design are shown in Table IV.

Table IV—Scaled Element Values for 2 GHz

f_o	n	L_M	C_M	C_T	L	L_n	C_n	C_C
300 MHz	5	32	216	200	28	28	8.1	2.7
2035 MHz	5	4.8	32.4	30	4.2	4.2	1.2	.40

The scaled values shown were derived from optimum experimental values at 300 MHz (example 1). Network Figure 21b was built on a metal plate and then inserted into a housing which held both the plate and a bandpass filter. Figure 27 shows construction details of the damped waveform generator. The required capacitors were cut from metallized ceramic materials and then soldered onto the metal plate. We found that ordinary copper or brass plates could not be used because the differential coefficient of linear expansion between the plate and the ceramic caused the brittle ceramic capacitors to break. A suitable plate material is sintered Copper Tungsten (Mallory 30W3 or equivalent). The plates were cut to size, machined, and then gold plated.* The components were then soft soldered on it.

*Nickel flash + 0.0002" gold plate. The material should be brought up to solder temperature before plating to outgas the material.

The bandpass filter used here was an edge-coupled, stripline filter of the type described in Ref. 18, Section 8.09. The damped waveform generator was placed as close as possible to the filter's input line to reduce line length which narrows the bandwidth.

The filter and the damped waveform resonator can be tested and optimized separately in 50 Ω systems and combined to produce the required multiplier.

A complete schematic and photographs of the multiplier are shown in Figures 28 and 29. We recommend that the dielectric material used in the filter have good electrical characteristics and dimensional stability. One such material is PPO.*

Figure 30 shows the damped ringing waveform output of this S-Band circuit. This output was then fed into the 50 Ω bandpass filter to remove the sidebands further.

Figure 31 shows the power input, power output curve for this multiplier. The overall pass band is shown in Figure 32.

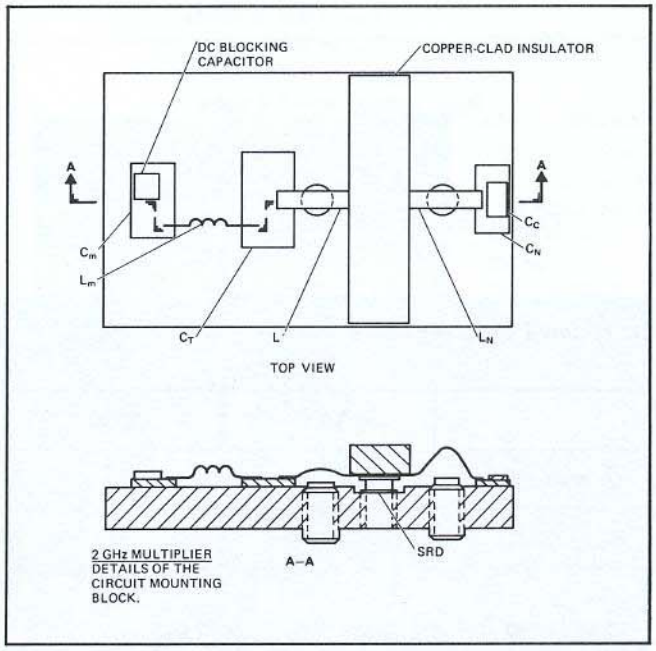


Figure 27. Circuit Layout of S-Band Multiplier

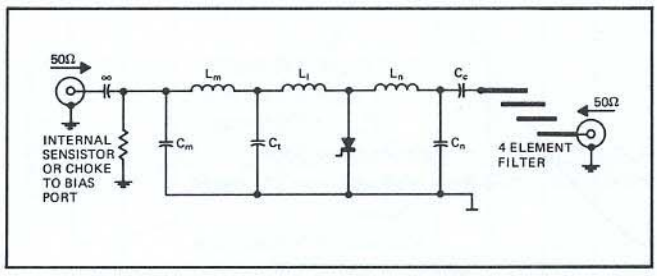


Figure 28. S-Band Multiplier Schematic
Multiplier Module—Open Housing
Overall Multiplier

*Copper-clad PPO (polyphenyl oxide—Trademark G.E. Co.)—Z-tron G; Polymer Corporation.

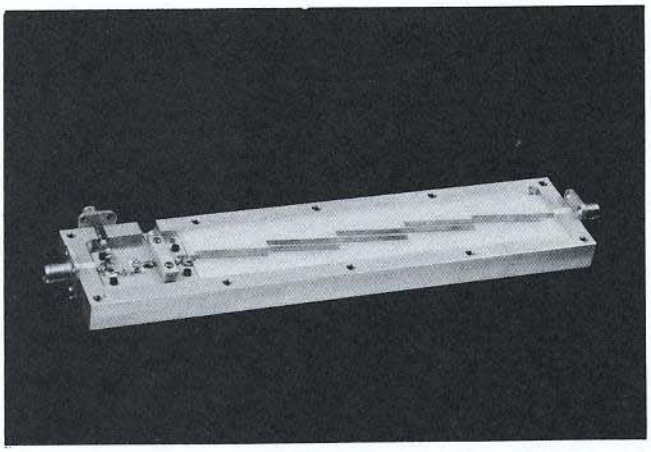
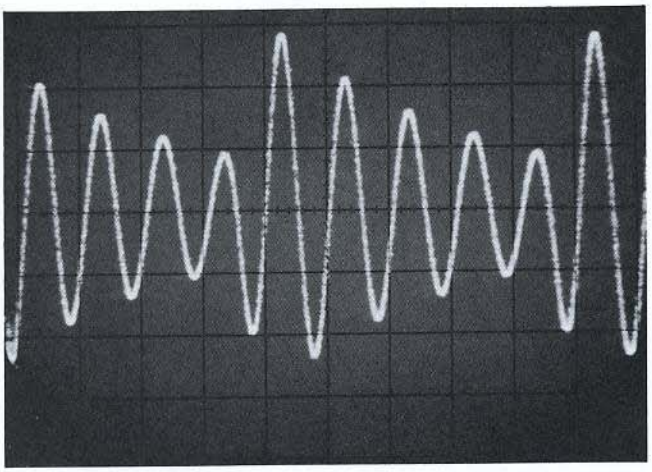


Figure 29. Photographs of S-Band Broadband Multiplier (X5)

P_{in} = 2.0 watts
P_{ref} = 0.016 watts
P_{out} = 1.05 watts
Efficiency = 53%
Bias Voltage = −2.9 volts
Scales
Vertical = 5 volts/cm
Horizontal = 500 picoseconds/cm
Frequency (Output) = 2.035 GHz



P_{in} = 2.0 watts
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Efficiency = 53%
Bias Voltage = −2.9 volts
Scales
Vertical = 5 volts/cm
Horizontal = 500 picoseconds/cm
Frequency (Output) = 2.035 GHz

Figure 30. S-Band Damped Waveform Generator (Bandpass filter removed—replaced by 50-ohm line)

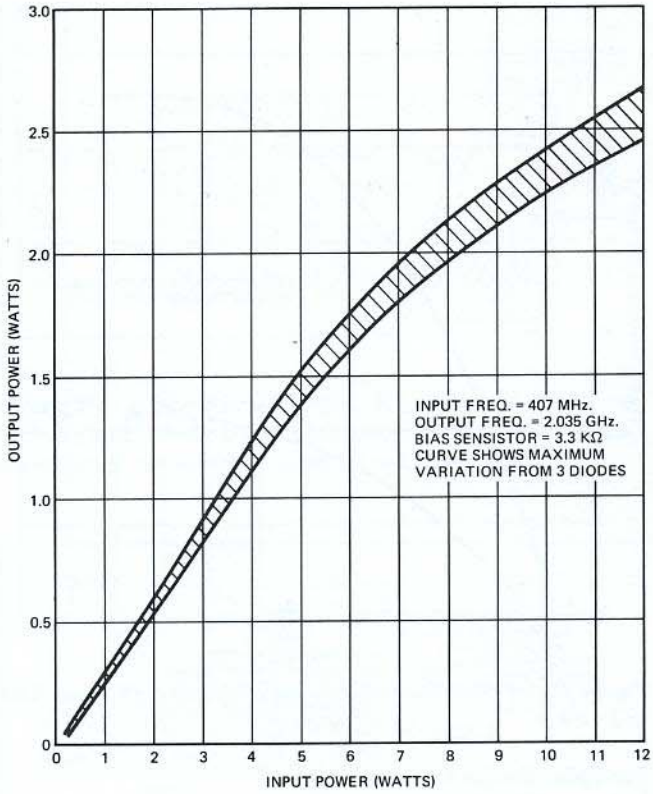


Figure 31. Power Output Reproducibility of S-Band Multiplier
(a) Output Power vs. Input Power

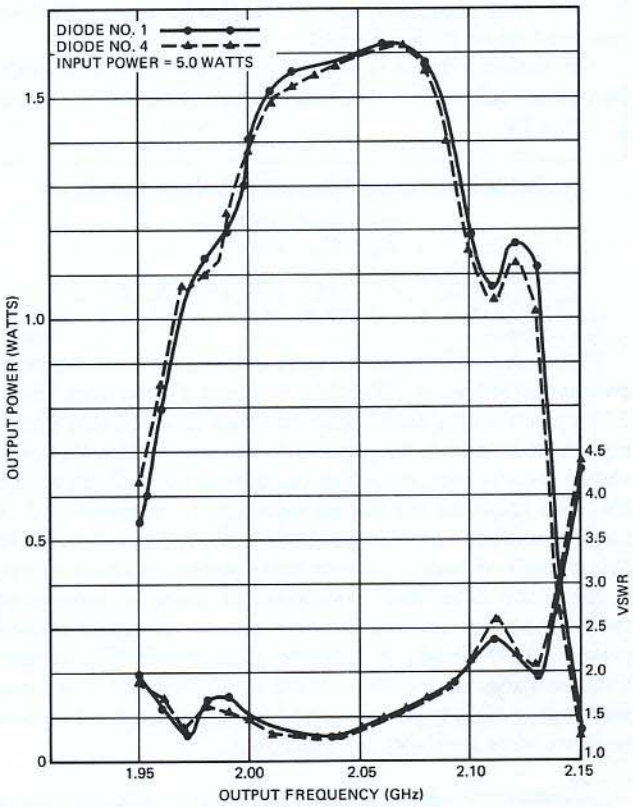


Figure 32. Output Power and VSWR vs. Frequency

Design Example 4: C-Band Multiplier

Multiplier Design Objectives

$f_{in} =$ 600 MHz
$f_o =$ 6000 MHz
$P_{in} =$ 4 watts
$P_o =$ 0.4 watt

Diode Selection

The diode selected for this application is the HP 0310. This diode is optimized for use at C band, and has a C_{VR} capacitance of 2 pF.

Impulse Generator Design

To operate effectively at 6 GHz, the required pulse width should be

$$83\ ps < t_p < 166\ ps$$

To minimize difficulties with element values, we chose $t_p = 140\ ps$. Choosing the larger pulse width has the effect of increasing the required drive inductance. The required element values are given in Table V.

Table V – Element Values, C-Band Impulse Generator

L	1.2 nh
C_T	50 pF
R_{in}	4.52
L_M	4 nh
C_M	17.6 pF

See Figure 15 (for circuit) and Table II formulas.

This circuit has been realized in much the same way as the Design Example 2. Figure 33 shows a cross-sectional drawing of the RF section of the impulse generator and the damped waveform generator.

The resulting impulse and damped waveforms are shown in Figures 34 and 35. The power out of the overall multiplier, including filter, at 6 GHz is shown in Figure 36. The bandwidth (65 MHz) of the multiplier shown in Figure 36 is just slightly less than the bandwidth of the filter, tested separately ($\approx$ 80 MHz).

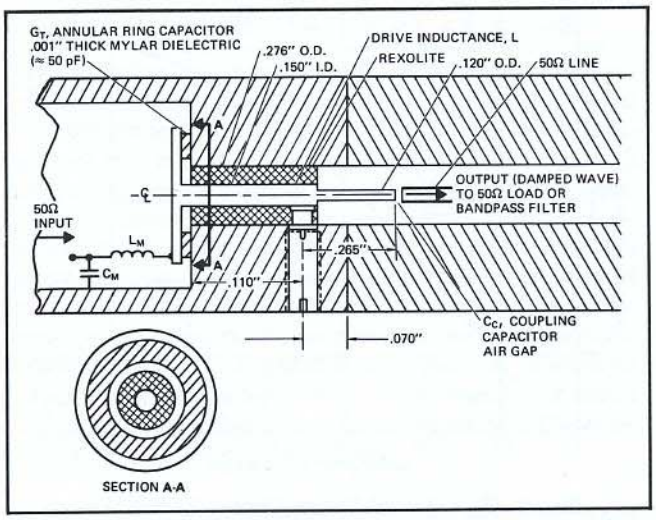


Figure 33. Cross-sectional Detail of C-Band Multiplier

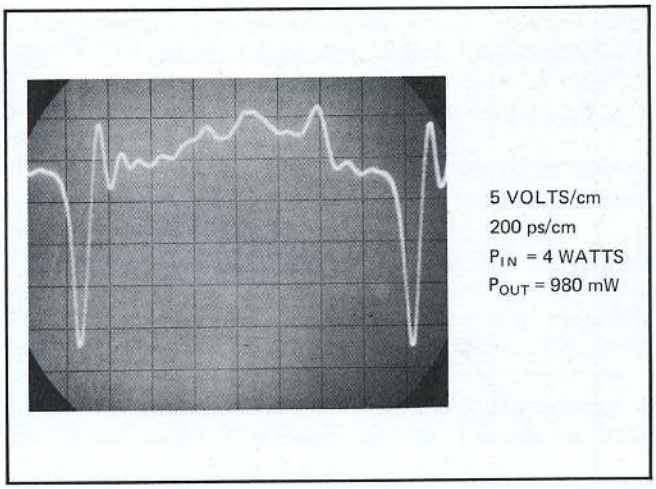


Figure 34.

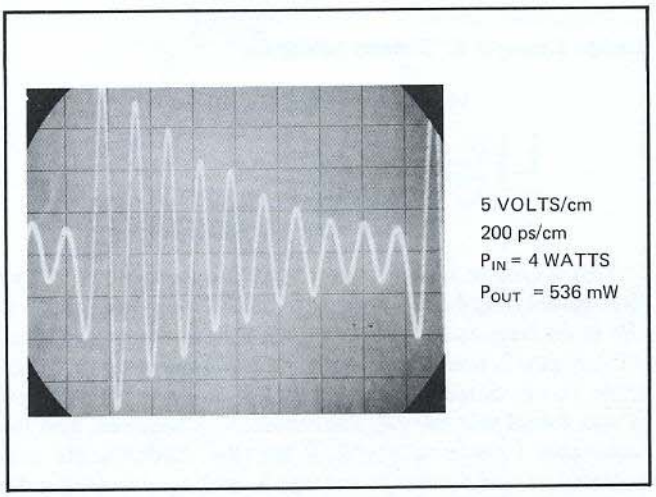


Figure 35. Damped Waveform

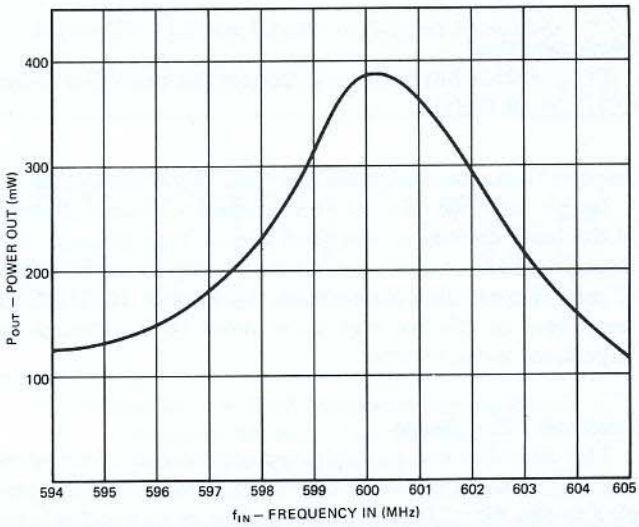


Figure 36(a).

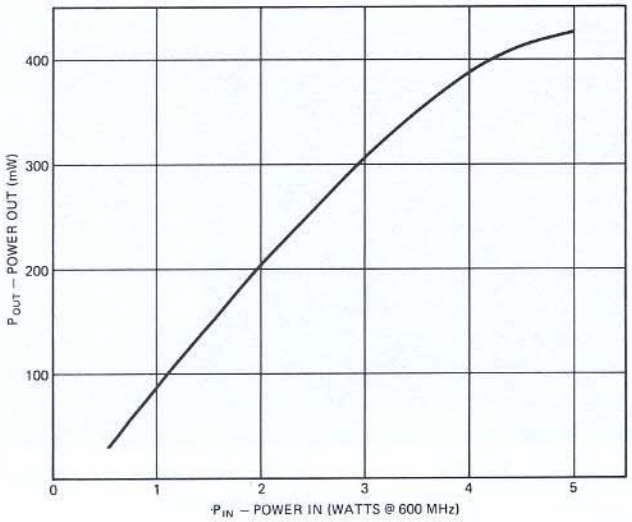


Figure 36(b).

Design Example 5: X-Band Multiplier

Multiplier Design Objectives

f_{in} = 2 GHz
f_{out} = 10 GHz
P_o = maximum available from diode (≃ 180 mW)

This example was evolved mostly experimentally. The first model built had two stubs to tune out the reactances at the input frequency. This is shown schematically in Figure 37. Lengths ℓ_1 and ℓ_2 were adjusted experimentally for maximum power output. Eventually, after testing many diodes, it was found that only ℓ_1 adjustment was required, and the adjustable ℓ_2 was removed. When the diode family was selected, it was further found that ℓ_1 no longer needed to be adjustable, This was the technique that was used to arrive at the X-Band multiplier design of Figure 38. The technique was also used successfully at S band in an early multiplier designed at HP (Ref. 10).

Diode Selection

The HP 0320 has been optimized for this multiplier design (X5, f_o = 10 GHz).

Impulse Generator Design and Damped Waveform Design

In this case, we used an experimental technique to arrive at the input circuit, as described above. The "ringing" line, from the diode to the point where it couples to the E-field of the bandpass filter is electrically $\lambda_0/4$ long at 10 GHz. The impedance of this line was set at about 30 Ω, although the impedance is not critical.

Bandpass Filter Design

Two quarter-wave, coaxial-coupled resonators formed the bandpass filter. The end of the "ringing" line is E-field coupled to this filter. Typical power output of this multiplier is shown in Figure 39.

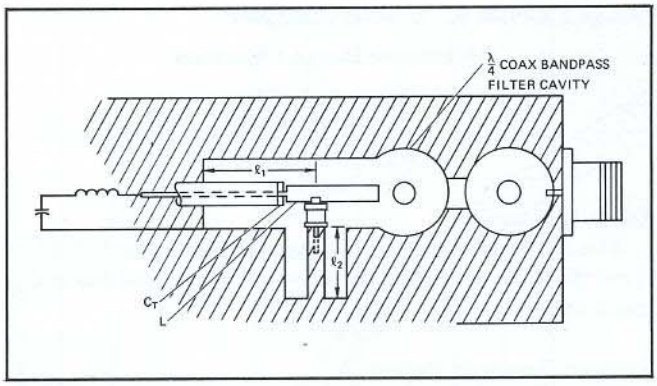


Figure 37. Schematic Diagram, Experimental Multiplier Stubs ℓ_1 and ℓ_2 were adjusted for optimum performance, and evolution of the design, Figure 38, was the result.

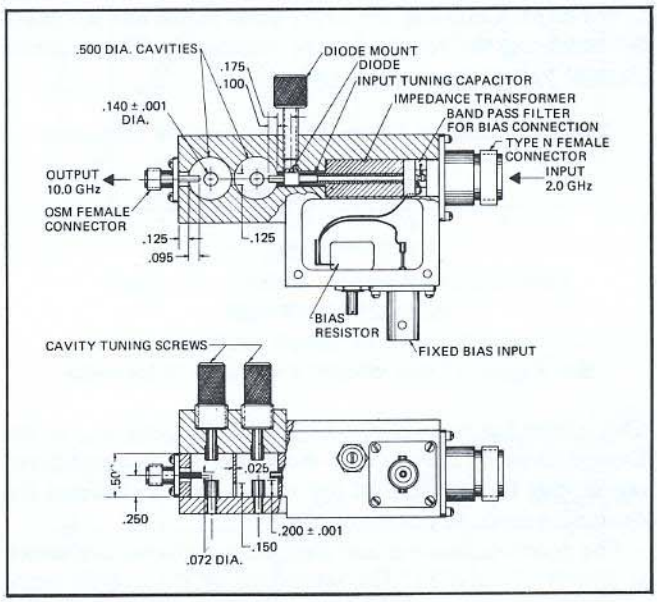


Figure 38. Mechanical and Electrical Layout of X-Band Multiplier

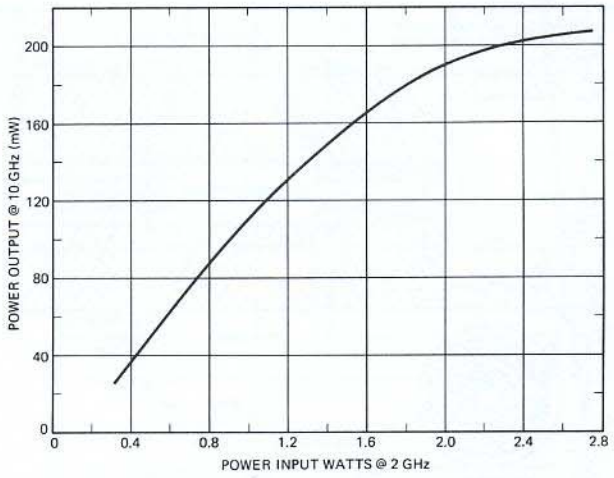


Figure 39. Typical Power Output Performance of HP 0320 Diode in Above Multiplier

IV. Hybrid Integrated SRD Modules

In this section we describe the hybrid integrated SRD circuits HP has recently introduced and their applications to CW multipliers. The Impulse Generator circuit (Figure 21a) has been hybrid integrated into a hermetically sealed, miniature, coaxial module (HP 33002/3/4/5, A and B versions).

When used as a comb spectrum generator, the modules are useful in the following applications:

1. Frequency and amplitude calibration of broadband receivers.
2. Generation of local oscillator power in totally coherent systems.
3. Frequency marking.
4. Generation of reference frequencies for phase-locking systems.
5. Sampling phase-lock systems as a gating pulse **or** as the local oscillator.

When used as a CW multiplier, the modules are useful in the following applications:

1. Generation of low power level phase-locking reference signals. For example:

   $n = 100$ at 10,000 MHz (0.4 milliwatt)
   $n = 60$ at 6,000 (2.5 milliwatts), etc.

2. Generation of local oscillator power from crystal-controlled low frequency inputs.
3. Driver for transmitter applications.

The purpose of this section of this note will be to give practical, illustrative examples of the applications of these hybrid integrated modules in high order, low power level (1 – 100 mW range) CW multipliers.

Why Hybrid Integration?

At frequencies where parasitic reactances are significant, the most practical construction method which will realize the impulse generator is hybrid integration. Series inductance is negligible ($\simeq$ 12 picohenries for the chip) and package capacitance does not exist.

There are also other reasons for integration:

1. As discussed earlier, thin film, RF capacitors are often required for C_T. These require protection from moisture and contamination the same way diodes do. Consequently, another "chip" can be used instead of a packaged device.
2. Small size, light weight, and high reliability are inherent in the design.
3. Hermetic sealing of the diode and its critical circuitry is made readily possible.
4. The most difficult part of the design has been taken care of by the semiconductor manufacturer. The applications of the modules to CW multiplier design require less engineering effort on the part of the user.
5. Allows the realization of some designs heretofore impractical; for example, X100 to 10 GHz, an example presented here, presents tremendous difficulties unless hybrid integrated circuits are used.

Device Description

Figure 40 shows the coaxial step recovery modules, their outline drawing, schematic and typical waveforms. Four SRD modules are available, tuned at input frequencies of 100 MHz, 250 MHz, 500 MHz, and 1000 MHz. These modules are also available in a 3 mm connector housing which contains a self-biasing dc return, on the output side (A versions).

When the module is driven by a sinusoidal frequency source and terminated at the output into 50 Ω, the output voltage consists of an impulse train, with a pulse height of 10-15 volts; a pulse width of 100-150 picoseconds, occurring at a repetition frequency equal to the input frequency. The input of the module is matched to 50 Ω at a 0.5 watt drive level. Higher input levels (to 0.75 watt) can be used but with an increase in input VSWR. Table VI shows the typical impulse output power of each of the four standard units.

Table VI – Typical Output Data for SRD Modules

Model No.	f_{in} (MHz)	t_p (ps)	E_p (volts)	P_{imp} (mW)
HP 33002A	100	130	14	26
HP 33003A	250	130	14	65
HP 33004A	500	130	14	130
HP 33005A	1000	130	10	130

$P_{in} = 0.5$ watt at f_{in} and 25°C

The 100-150 psec pulse width makes these modules most useful for generation of a frequecny comb spectrum or for multipliers whose output frequency is in the 4-10 GHz range.

Application as a Frequency Comb Generator

For use as a frequency comb generator, the SRD module is simply connected to a source of CW power and the output of the module is terminated by the 50 Ω load where the spectrum is to be delivered. This is shown in Figure 41.

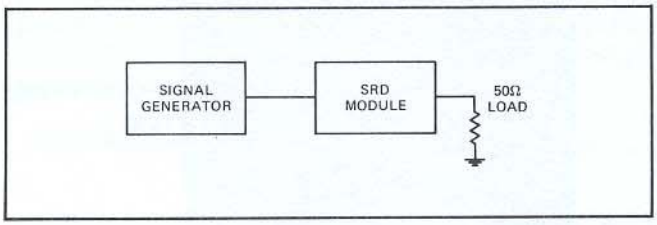


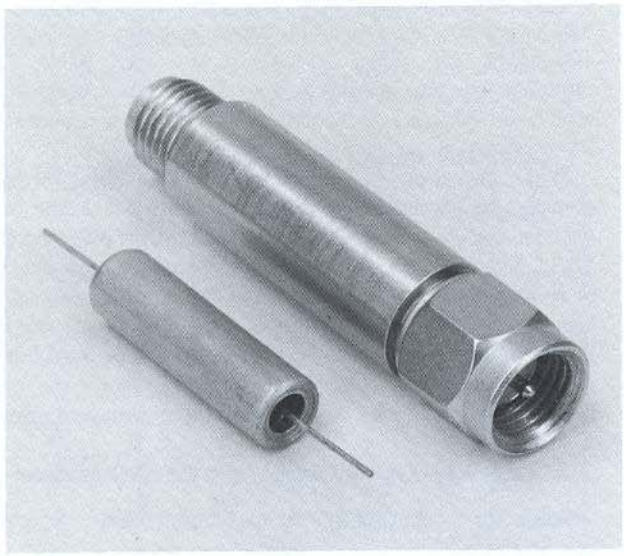
Figure 41. Connection as a Comb Generator

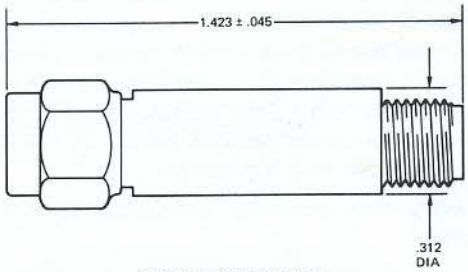
A typical output spectrum that will be obtained is shown in Figure 40. A bandpass filter may be used to limit the output frequency range as desired. In these applications, an extremely flat spectrum can usually be obtained. For closer spacing of the comb frequencies, low input frequency SRD modules can be obtained on special order, down to 25 MHz. Modules, at non-standard input frequencies, are available on special order.

Applications, SRD Modules as CW Multipliers

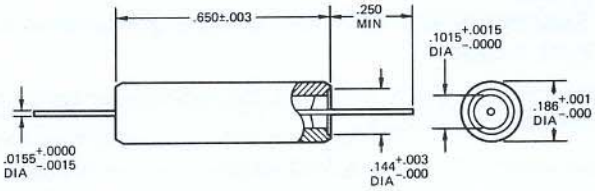
The SRD module may be used very effectively as a low-level single-frequency multiplier in the 4-10 GHz output frequency range.* A block diagram of a CW multiplier using

*Wider pulse width modules, for use at lower output frequencies, are available on special order.

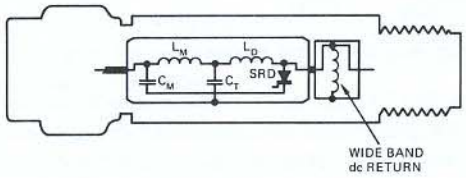




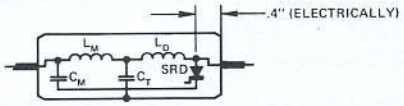
33002B/3B/4B/5B



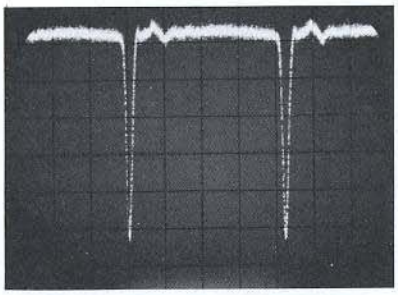
33002A/3A/4A/5A



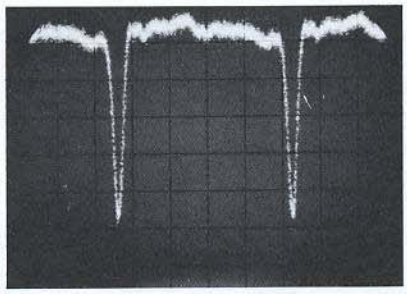
Electrical Schematic of "A" Versions



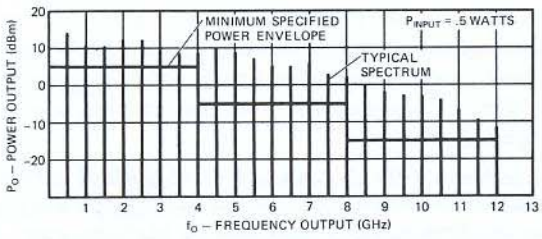
Electrical Schematic of "B" Versions



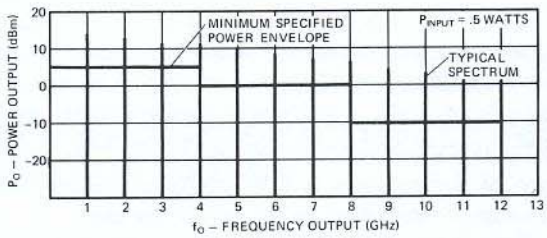
Impulse Waveform 33004A/B (500 MHz)



Impulse Waveform 33005A/B (1000 MHz)



Spectrum Envelope of 33004A/B (500 MHz)



Spectrum Envelope of 33005A/B (1000 MHz)

Figure 40. Device Description

a standard SRD module is shown in Figure 42. The module is coupled to a bandpass filter through a resonant network. The resonant network may be any one of those shown in Figure 6. The bandpass filter may be any one of those

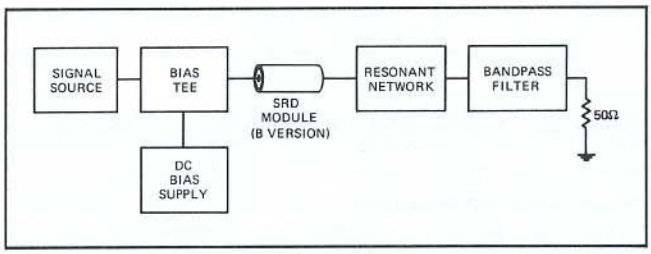


Figure 42

shown in Figure 9. Prototype multipliers of each of the types of Figures 7 and 8 have been built using modules. Examples of these designs will be given below.

Example 1: The Quarter-Wave Coupled Multiplier

Perhaps the simplest way to make a multiplier is as shown schematically in Figure 43. A probe is soldered onto the output end of the module. The module is then placed so that the probe, E-field couples to a quarter-wave bandpass filter. The length of the

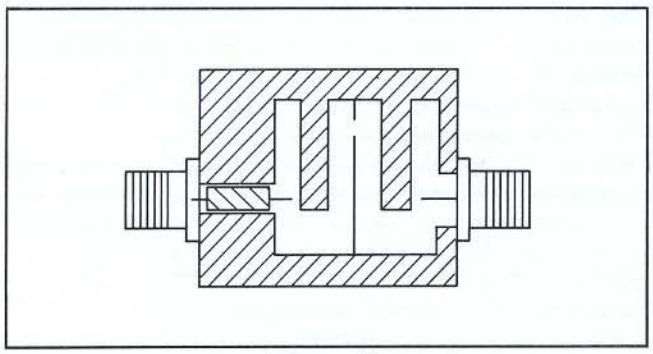


Figure 43

length of the probe, external to the module, together with the 0.4″ internal electrical distance to the diode (Figure 40) make up the $\approx \lambda_0/4$ ringing line. The line capacitively couples to the bandpass filter, as shown in Figure 7C.

A detailed drawing of cavity and probes for 6 GHz output frequency is shown in Figure 44. Any one of the four modules, with added probe, will form a 6 GHz multiplier.

This technique was used to build a variety of multipliers at various output frequencies from 4 to 10 GHz. The input power in all cases was 0.5 watt. The input was swept, when possible, and pass bands of two of these multipliers are shown in Figures 45 and 46. Each of these examples was swept around 450 MHz, using a module whose center frequency was 500 MHz. This accounts for the relatively high reflected power, but also illustrates the versatility of the module.

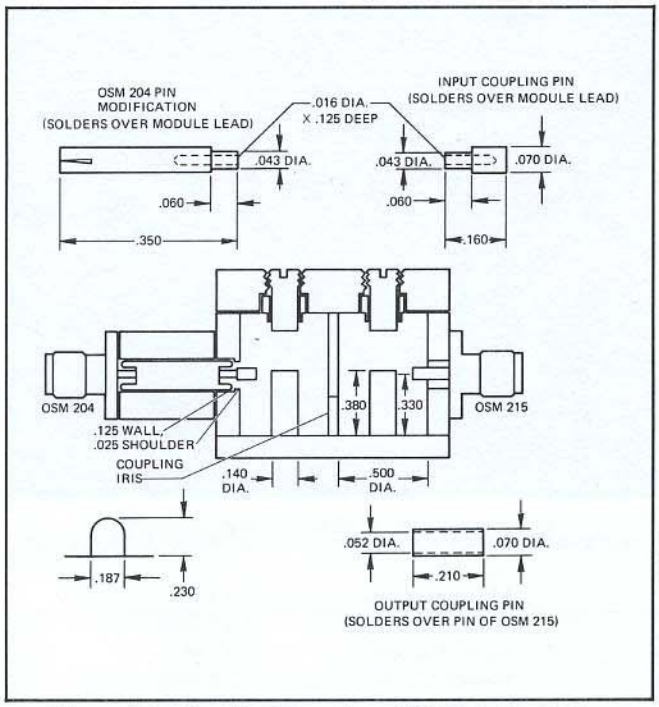


Figure 44. Detailed Drawing of 6 GHz Multiplier

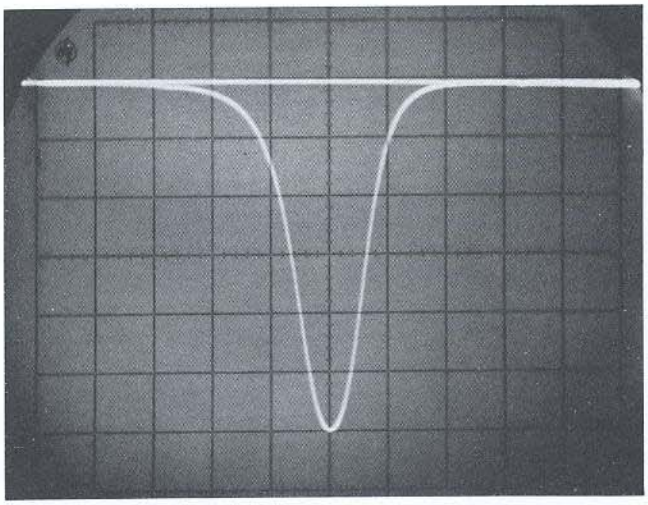
As further illustration of the versatility and broad applicability of these modules in low-level multiplier applications, a variety of multipliers were made using 4, 6, 8, and 10 GHz output bandpass filters and the four modules (at 100, 250, 500, and 1000 MHz).

The performance of eight multipliers made in this way is summarized in Table VII. All of these multipliers were stable at 0.5 watt drive with a short circuit of any phase on the output.

Table VII—Performance of Eight Module-Filter Combinations as CW Multipliers

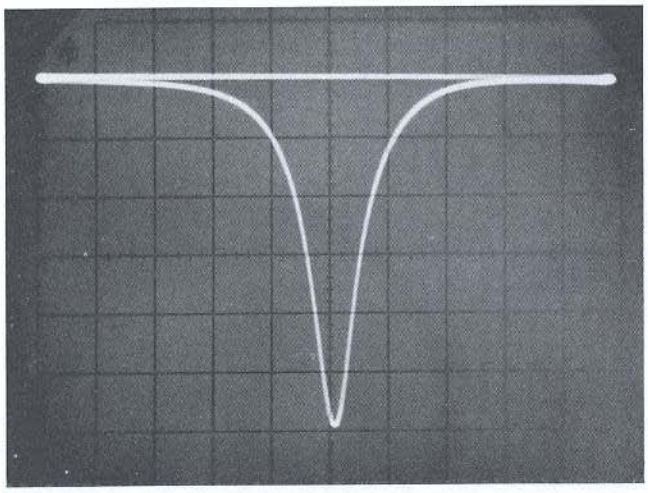
Each multiplier tuned by adjusting probe depth, and tuning filter. Self-bias brought to module on input side through bias tee designed as in Section II.

HP Model	f_{in}/f_0	6000 MHz	10,000 MHz
HP 33002B	100 MHz	$n = 60$ $P_o = 2.6$ mW $BW = 30$ MHz	$n = 100$ $P_o = 0.5$ mW $BW = 24$ HMz
HP 33003B	250 MHz	$n = 24$ $P_o = 5$ mW $BW = 34$ MHz	$n = 40$ $P_o = 2$ mW $BW = 23$ MHz
HP 33004B	500 MHz	$n = 13$ $P_o = 13.2$ mW $BW = 35$ MHz	$n = 20$ $P_o = 7.2$ mW $BW = 20$ MHz
HP 33005B	1000 MHz	$n = 6$ $P_o = 10.5$ mW $BW = 36$ MHz	$n = 10$ $P_o = 10$ mW $BW = 25$ MHz



SWEPT FREQUENCY RESPONSE

Multiplication:	X13
Output Frequency:	5.85 GHz
Input Frequency:	450 MHz
Power Output:	13.2 mW
Power Input:	0.5 watt
Power Reflected:	5 dB down
Bias Resistance:	130 ohms
Bandwidth (3 dB):	35 MHz



SWEPT FREQUENCY RESPONSE

Multiplication:	X22
Output Frequency:	9.928 GHz
Input Frequency:	452 MHz
Power Output:	7.2 mW
Power Input:	0.5 watt
Power Reflected:	8.5 dB down
Bias Resistance:	55 ohms
Bandwidth (3 dB):	20 MHz

Figure 45. C-Band High Order Multiplier Characteristics

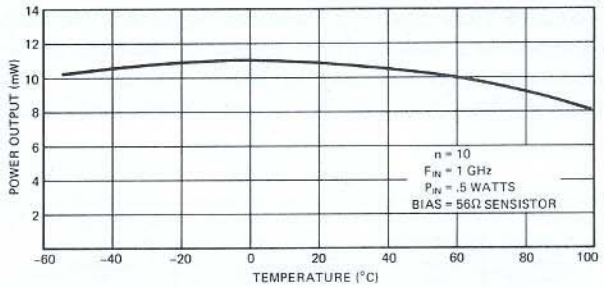


Figure 46. X-Band High Order Multiplier Characteristics

Temperature Compensation

The bias resistance required for self-bias is directly proportional to the diode lifetime. The lifetime is the only significant parameter that changes as a function of temperature over normal operating temperature ranges (Ref. 1). The rate of change of SRD lifetime is + 0.5% to + 0.7%/°C. This is closely matched by the rate of resistive change of a silicon resistor (sensistor). If a multiplier has a reasonably broad range of bias resistance, the multiplier can be temperature compensated by simply using a sensistor to develop the bias voltage instead of a resistor.

Typical temperature performance of a compensated 10 GHz times 10 SRD module multiplier is shown in Figure 46. Compensation was by a sensistor and by using Invar center conductors in the cavities of the 2-cavity output filter. The Invar center conductors were required because of the frequency change caused by the change in length over temperature. This is important primarily in narrowband (<1%) filters.

Example 2

Another method of coupling the module to a bandpass filter is shown in Figure 47. The $\lambda_o/2$ resonant network of Figures 6 and 8 is used. The electrical length must take into account the 0.4" internal length in the module (Figure 40).

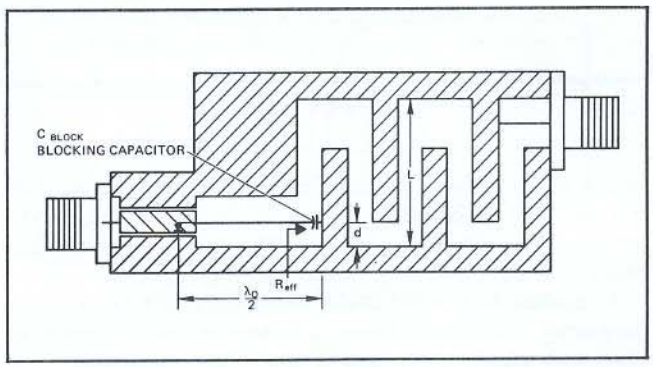


Figure 47. SRD Module Coupled to Interdigital Filter A $\lambda_0/2$ line drives the interdigital filter by coupling into a low impedance "tap point" (Ref. 15). The blocking capacitor is chosen to form a series resonance to ground at $1.25 f_i$.

The $\lambda_0/2$ line must terminate in a low resistive impedance, R_{eff}, that will give a loaded $Q \approx (\pi/2)n$. (See Figure 6b.) One convenient way to do this is to "tap in" on the first element

of the interdigital filter (see Dishal, Ref. 15). The height above ground, d, at which to tap the $\lambda_o/2$ line into the filter is found as follows:

$$Q_l = \frac{\pi}{2}\frac{Z_o}{R_{eff}} = \frac{\pi}{2}n$$

$$\therefore R_{eff} \cong \frac{Z_o}{n}$$

where Z_o = characteristic impedance of the ringing line.

Dishal (Ref. 15, equation 8) gives an expression for the loaded Q of the first element of an interdigital filter when a resistor, R, is tapped onto the first resonator, d inches above the ground plane. We shall assume that we can replace his R by R_{eff}, and solve for the appropriate "tap" point accordingly; i.e.,

$$Q_1 = q_1\frac{f_o}{\Delta f} = \frac{\pi}{4}\frac{R_{eff}}{Z_{01}}\left[\frac{1}{sin^2\frac{\pi}{2}\frac{d}{L}}\right]$$

where

Q_1 is the required first element loaded Q
q_1 is the normalized design from tables (Reference 21; p. 218 for example) ($q_1 = 1.34$ for a 4 element, 0.1 dB ripple design)
Δf is the required filter 3 dB bandwidth
$L - \lambda_0/4$ (see Figure 47)
d – height above ground plane to "tape in" point

The remainder of the filter design (the coupling coefficients, and output loading) follow Ref. 15.

In order to avoid dc short circuiting the SRD, a blocking capacitor is needed at the tap point (Figure 48). The value of this capacitor must be chosen with the stability criterion in mind. That criterion was stated earlier, that no short circuit resonances should appear across the diode at frequencies less than f_{in}. To avoid problems of this sort, set the resonant frequency of C_{BLOCK} and the inductance of the $\lambda_o/2$ line such that

$$f_{SR} \cong 1.25\, f_{in}$$

where

$$f_{SR} = \frac{1}{2\pi\sqrt{L_{\lambda 0/2}\cdot C_{BLOCK}}}$$

This results in the following value of C_{BLOCK}:

$$C_{BLOCK} \cong \frac{n}{30\, f_i Z_o}$$

An example of a multiplier built this way is given next. The example uses a non-standard module, to illustrate what changes in pulse width can do. Namely, by broadening the pulse, it is possible to get higher power output at lower frequencies. Multipliers using the standard modules may also be designed in this way.

Special Multipliers Using SRD Modules

The SRD modules used in the examples of Table VII all had the same output pulse width (130 ps) and were most optimum for multipliers in the 4-10 GHz output frequency range. SRD modules using different SRD chips (i.e., 0300, 0310, or 0330 types) are easily optimized for other frequency ranges and are available on special order. The following examples illustrate what can be achieved in terms of performance stability, size, and special characteristics.

S-Band Interdigital Filter Multiplier

Characteristics

Multiplication:	X20	Bandwidth (3 dB) = 30 MHz
Output Frequency:	2.05 GHz	
Input Frequency:	102.5 MHz	
Power Output:	90 mW	
Power Input:	1 watt	

The SRD module for this multiplier was designed for a pulse width of 350 psec. The output filter is a 5-section interdigital type and the SRD module is coupled via a $\lambda_o/2$ line, built in microstrip form, described above. The multiplier was stable for all phases of a short circuit on the output. A photograph of the multiplier is shown in Figure 48. The waveforms obtained in the coupling line during the tuning operation are shown in Figure 49, a and b. Figure 49a shows the waveform when the first element of the filter is shorted. This establishes the resonant frequency of the coupling line.

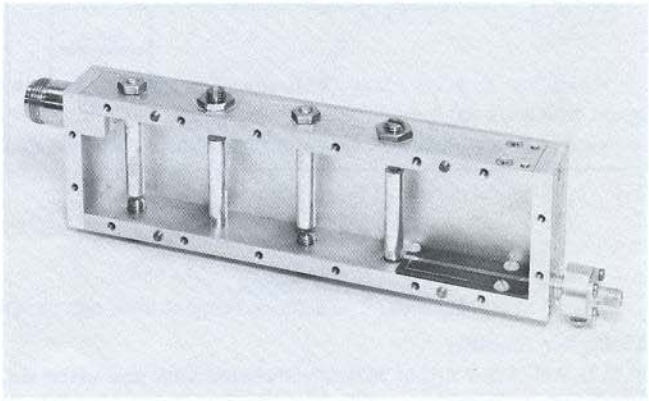
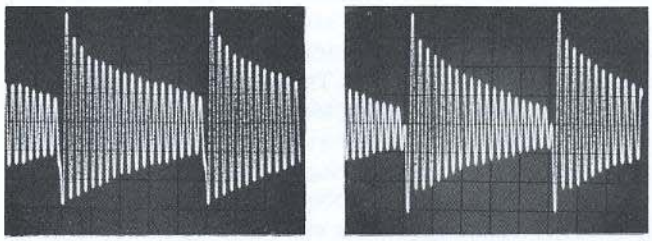


Figure 48. An S-Band Multiplier Using an Interdigital Filter

Figure 49b shows the waveform after the filter has been tuned up. The waveforms are different only by the additional loading introduced by tuning the filter.



(a) FIRST ELEMENT OF FILTER SHORTED

(b) FINAL WAVEFORM (IN FIRST SECTION) OF TUNED-UP MULTIPLIER

Figure 49. Waveforms - first resonator loaded and unloaded.

Tune-up of the multiplier is aided by using a modified Dishal technique (Ref. 22).

1. Set up the multiplier as in Figure 50. (The tune-up starts from the output side.) Set signal generator to band center (output frequency).

2. Short circuit all resonators.

3. Move slotted line probe to minimum.

4. Tune output resonator to maximum, (n-1) to minimum, etc., up to but not including first resonator.

5. Set up as multiplier; turn on input power at $f_{in} = f_o/n$; tune first resonator for maximum power output.

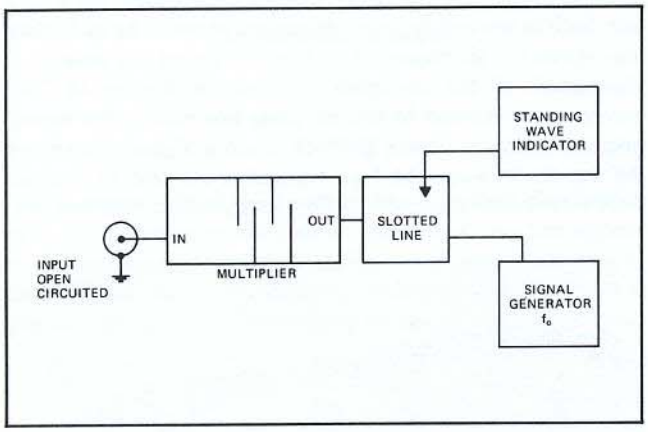


Figure 50

V. Special Topics

Multiplier Stability

It is well known that multiplier chains can, and often do, break into parametric oscillations. In fact it was possible to measure parametric gain in the X5, S-band multiplier, Figure 29, Section III. The gain was measured at the input port and was found to be due to the presence of a negative resistance. Under some conditions, the gain can become infinite, leading to oscillations.

Figure 51a shows the setup that was used to deliberately generate parametric oscillations. The high pass filter had a sharp cutoff at 100 MHz. A 380 MHz, low-level signal was fed into the input of the multiplier through the decoupled arm of a directional coupler. The reflected 380 MHz power was measured on the decoupled arm of the second coupler. The reflection coefficient, for a net negative input resistance, is greater than one, thus giving a power gain between incident and reflected waves. Negative input resistance in a parametric device appears at either the signal frequency or at the idler frequency, depending upon the terminations.

As long as the signal and idler behave as $f_s + f_i = f_p$, the negative resistance can appear at either one if the other is resonated properly.

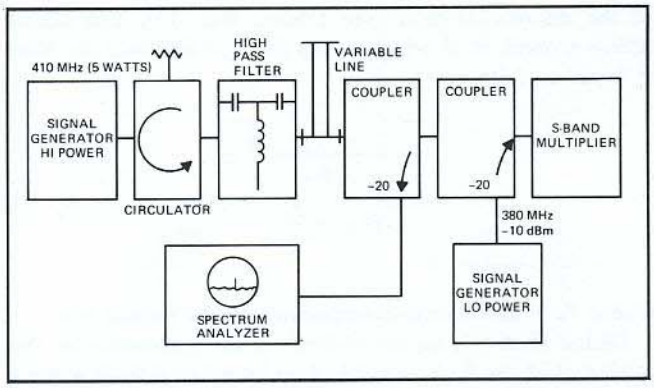


Figure 51a. Test Setup for Investigation of Parametric Effects

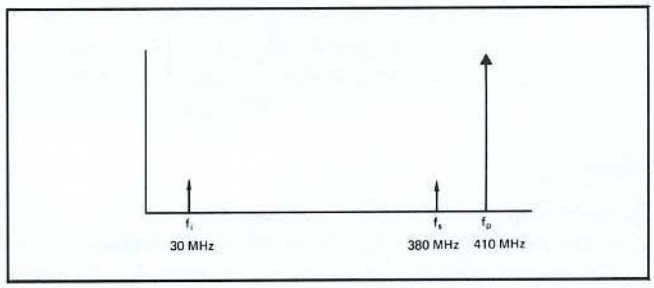


Figure 51b. Frequency Spectrum in Parametric Investigations

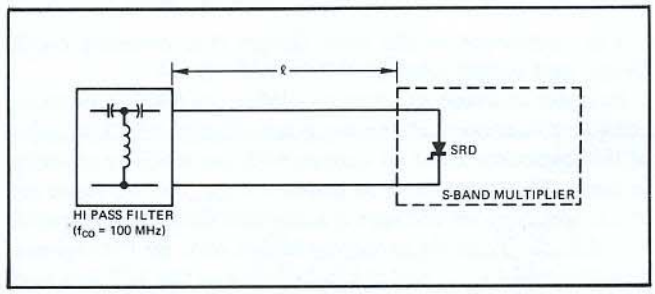


Figure 52. Idler Configuration Used To Deliberately Induce Parametric Oscillations

In Figure 51b, an "idler" was being formed at 30 MHz by the length of line between the multiplier and the high pass filter (Figure 52). The frequency at which high gain appears increased with ℓ. This is consistent with the diagram of Figure 51b.

In the vicinity of the frequencies where the multiplier broke up, the parametric gain was very high, 20-35 dB. A slightly larger "leak signal" would cause the multiplier to break up. The spectrum signature of the multiplier in self-oscillation was indistinguishable from the spectrum signature when it was driven into oscillation by a "leaked" in signal.

Of course, parametric oscillations are **not** wanted in multipliers. How does one go about eliminating them?

Based on the description of parametric gain in the above paragraphs, one can speculate that if all possible idler resonances could somehow be removed, perhaps there would be no negative resistance anywhere, and hence no possibility of going into parametric oscillations. Accordingly, one would

want to see no short circuit resonances at any frequency across the diode. Resonances between dc and f_{in} are especially important as they tend to cause the highest gain (largest negative resistance) and, therefore, the greatest instability.

Stability and the Bias Circuit

Bias circuits as in Figure 53a are frequently the cause of parametric instabilities. When the Q of the network is high, a series resonance between L_{CH} and C_{bypass} leads to low frequency oscillations if the series resonance may be "seen" from the diode in the multiplier circuit. Elimination of the bypass capacitor, C_{bypass}, frequently eliminates the oscillation.

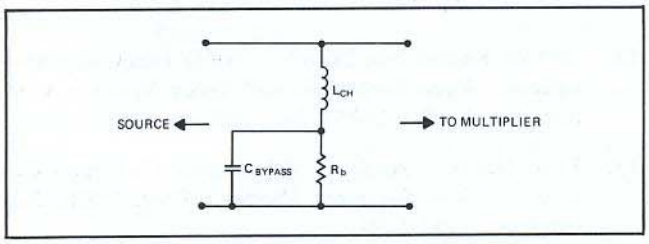


Figure 53a. A bias circuit arrangement which frequently causes parametric instabilities.

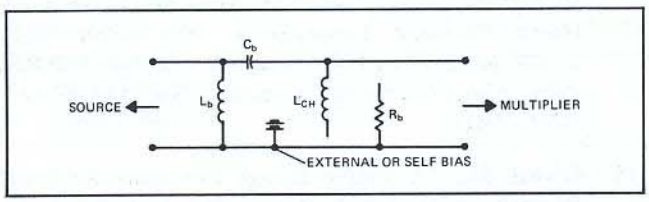


Figure 53b. A bias circuit which improves multiplier stability by avoiding low frequency parametric effects.

To avoid unnecessary interaction with source circuitry, the high pass filter (53b) discussed in Section II is helpful. The high pass circuit has also been found to be an excellent way to introduce bias, in many cases stabilizing the multiplier (Figure 15).

To summarize, it was experimentally shown that the step recovery diode multiplier can act as a negative resistance parametric amplifier under some conditions. When a high Q series resonance (f_{SR}) is placed across the diode between 0 and f_{in}, a high gain condition may be set up at $f_{in} - f_{SR}$; this gain may be high enough to produce oscillations.

The converse has also been shown to be true; by avoiding high Q, series resonances (such as often occur with bias circuitry) stability can be markedly improved. Multipliers having stable outputs with a short circuit at any phase angle on the output have been built using this approach. Work is continuing to determine the necessary driving impedances to guarantee stable multiplier operation with any driver output impedance.

Multiplier Phase Noise Characteristics

Measurements have been made to determine the excess phase noise introduced by step recovery diode multipliers. To measure excess multiplier noise "directly," the technique shown in Figure 54 was used. Here, a 100 MHz crystal

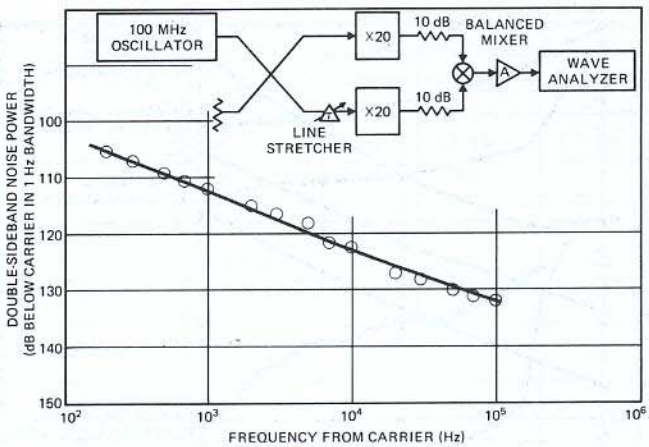


Figure 54. Excess Multiplier Phase Noise Measurement

oscillator was used to drive two identical "times 20" multipliers. The line stretcher was used to adjust the relative phase angle of the 2 GHz signals into the mixer to be 90° (indicated by zero dc out). The multiplier noise contribution of the 100 MHz oscillator is cancelled out and only the excess multiplier noise of the multipliers (assumed equal) is measured. The results are plotted as double sideband noise power in dB below the carrier normalized to a 1 Hz bandwidth.

In Figure 55, two oscillator-multiplier combinations were used, in which one oscillator had a "Varicap" in series with the crystal to permit frequency control. This oscillator was phase-locked to the other in a 1 Hz bandwidth loop. The circles indicate measured points in which the oscillators were phase-locked via the 100 MHz mixer and the triangles indicate points where the 2 GHz mixer was used. The dotted curve is the level expected for an ideal "times 20" multiplier.

To give a comparison of the noise output of the SRD multiplier, the data of Figure 56 at 2 GHz was scaled to 4 and 6 GHz for comparison with previously published data (Ref. 23). The noise measured is typically lower than single-cavity klystrons, but higher than two-cavity klystrons out to $f_{in} \approx$ 100 kHz. Klystron noise reduces with increasing modulation frequency, noise in solid state chains increase with f_{in} because of amplifier noise.

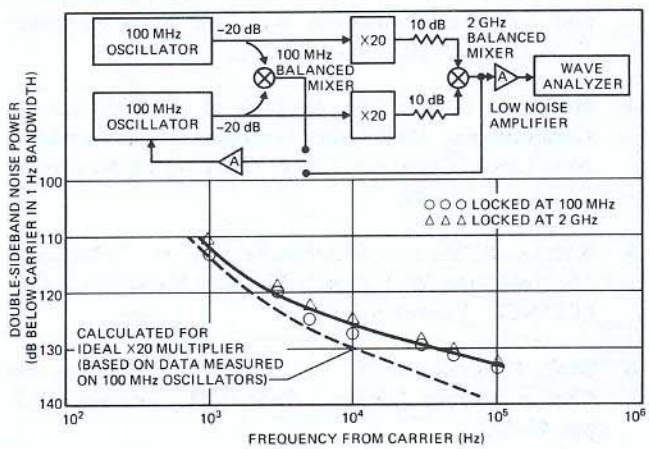


Figure 55. Phase Noise Measurement

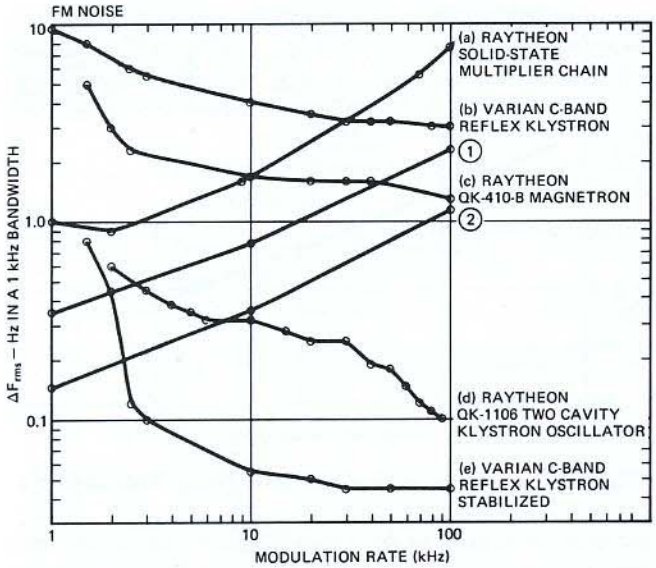


Figure 56

Reprinted from Johnson et al. (Ref. 23). "FM Noise Performance of Solid State X40, X60 Multipliers at 4 GHz and 6 GHz."

Data extrapolated from 2 GHz measured data for comparison with previously published data.

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APPENDIX A

Efficiency of SRD Multipliers

There are four important losses to account for in the generation of the impulse.

1. Recombination losses ($\omega\tau \neq \infty$).
2. Finite matching circuit losses ($Q_u \neq \infty$).
3. Transition losses (some energy is lost while the diode is opening).
4. R_s losses.

After the impulse has been generated, it has an output power of P_{imp}; where:

$$P_{imp} = \pi\zeta E_p^2 f_{in} C_{VR} = P_{in}\xi_{CW \rightarrow imp} \tag{1}$$

The impulse is subsequently converted to CW at $f_o = nf_{in}$. There are two important losses in this process:

1. R_S loss—the pulse travels through R_S approximately $2n$ times per input cycle, causing some loss due to voltage division each time.
2. Finite output filter loss—Q_u's of last filter $\neq \infty$.

Overall multiplier efficiency is then found from

$$P_{out} = (L_{filter}) * (Efficiency_{imp \rightarrow CW}) * P_{imp} \tag{2}$$

or

$$P_{out} = P_{in}\,[L_{filter} * \xi_{imp \rightarrow CW} * \xi_{CW \rightarrow imp}] = \xi_{overall} * P_{in} \tag{3}$$

Impulse Generator Efficiency

Of the four losses above, only transition loss and R_S losses will be discussed here. The lifetime losses can be minimized by keeping $\omega\tau >> 1$. Circuit losses are small because $Q_L \simeq 1$.

The remaining losses, transition loss and series resistance loss, will be calculated separately—as partial efficiencies—so that

$$\xi_{imp \rightarrow CW} = \xi_{due\ to\ R_s} * \xi_{due\ to\ transition\ losses} \tag{4}$$

Transition Losses

Just prior to the "snap" of the diode, the diode and circuit equivalent are shown in Figure A1.

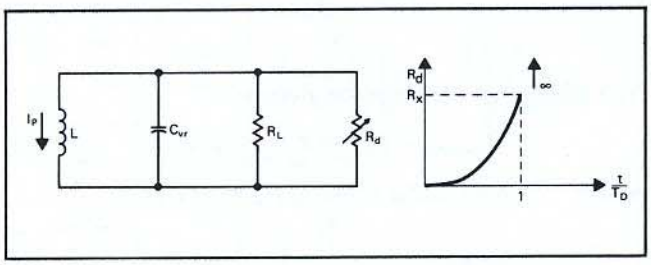

Figure A1. Equivalent Circuit While Transitioning

The R_d of Figure A1 represents the equivalent behavior of the diode beginning at the time when the charge at the edges of the I-layer has gone to zero.* Between this time and $t = T_D$, the resistance behaves as $R_D \cong (t/T_D)^5 R_X$ (See Ref. 14).

where

$$R_X = \frac{V_{BR}}{5C_{VR}\,(pF)} \tag{5}$$

*Leaving only the charge in the center to diffuse out; it does so with time constant T_D, causing the transition loss mechanism.

The loss during this time, assuming constant extraction current, I_p is

$$P_{Trans} \cong I_p^2 R_{Tr} \tag{6}$$

where

$$R_{Tr} = \frac{V_{BR}}{30C_{VR}\,(pF)} \tag{7}$$

The loss then may be written in ratio to the P_0 (also expressible in terms of I_p) as an efficiency

$$Eff_{due\ to\ Trans} \cong \frac{1}{1 + \dfrac{N\,V_{BR}}{t_p\,(ps)}} \times 100\% \tag{8}$$

Series Resistance Loss (Impulse Generator)

In Reference 1, the expressions for the current in the Impulse Generator were derived. It was shown that the current in the conduction cycle was shown to be $i_{IN}(t)$ (Figure A2) where:

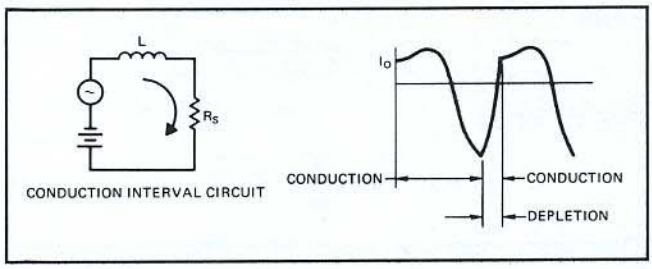

Figure A2. Equivalent circuit-conduction interval

$$i_{IN}(t) = I_o + \frac{E}{\omega L}\,[\cos\alpha - \cos\,(\omega t + \alpha)\,] - \frac{V + \phi}{\omega L}\,\omega t \tag{9}$$

The loss due to finite forward resistance will be estimated by perturbation, by addition of a small R_S (relative to L, R_S is assumed small [an approximation good to 10% for $R_S < 1/2\ \omega L$ or so]). The expression (9) must be put into terms of a common drive, e.g., $E/\omega L$.

The bias condition was originally established (Ref. 1, Equation 10) by forcing i to be maximum at the instant of the snap; $L\ di/dt\ |_{t = t_1} = 0$. Then:

$$V + \phi = E\,\sin\,(\alpha - \pi/n) \tag{10}$$

Also, it was shown the $q(t_1) = 0$, (Ref. 1, Equation 7), thus relating $E/\omega L$ and I_0.

$$I_o = K\left(\frac{E}{\omega L}\right) \tag{11}$$

where

$$K = \left(\frac{m}{2} + \frac{1}{m}\right)\sin\,(\alpha - \pi/n) - \frac{\sin\alpha}{m} - \cos\alpha \tag{12}$$

where

$$\begin{cases} m = 2\pi - \pi/N \\ N = \dfrac{1}{2f_{in}t_p} \end{cases}$$

Then $i_{IN}(t)$ is entirely expressed in terms of (E/L), m, N, and α.

The power lost in the series resistance (during impulse formation) is primarily during the conduction interval. Ignoring the impulse interval (during which the current is smaller), which is of duration $T/2N$, causes errors of the order $1/2N$. The loss is the rms current squared times R_S, or:

$$P_{Loss} = \frac{R_S}{t_1}\int_0^{t_1} i^2_{cond}\,(t)\,dt + \frac{R_S}{n/\omega}\int_{t_1}^{2\pi/\omega} i^2_{depl}{}^{dt} \qquad (13)$$

disregard at this stage

From (9), (10), and (11), this expression is a function times $(E/\omega L)^2$; fortunately, the output power can also be expressed the same way, leading to cancellation of the common $(E/\omega L)^2$ terms.

From (16) (Ref. 1)

$$P_o = 1/2\ LI_o^2\ [G^2 - 1]\ f_{in} \qquad (14)$$

where

$$G = \exp\frac{\pi\zeta}{\sqrt{1-\zeta^2}}$$

from (4) we get

$$P_o = 1/2\ LK^2\left(\frac{E}{\omega L}\right)^2 f_{in}\ [G^2 - 1] \qquad (15)$$

The efficiency due to R_S losses, 100% if $R_S = 0$, is now given by

$$\xi_{RS\ contribution} = \frac{1}{1+\dfrac{P_{Loss}}{P_o}} * 100\% \qquad (16)$$

where P_{Loss} and P_o are given in terms of $(E/\omega L)^2 * f(N, m, \alpha)$.

Total Impulse Generator Efficiency

The efficiency of the impulse generator circuit is given by the product of the efficiencies of equations (8) and (16).

Impulse to CW Conversion

The series resistance is important also in determining the conversion loss imp CW. The equivalent impulse output generator (Figure 4) is shown in Figure A3, with a resonant output network ($\lambda/4$ line). The diode series resistance has been added to account for the power lost there in the impulse to CW conversion process.

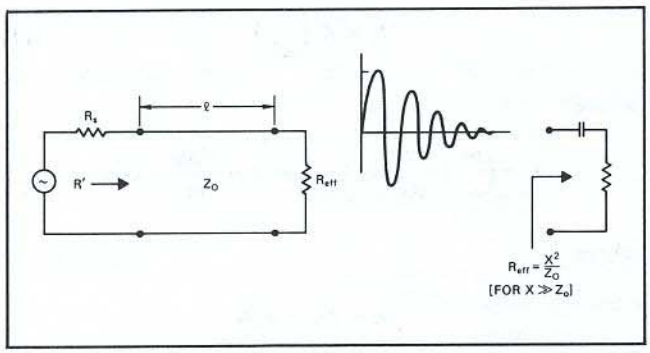

Figure A3. Equivalent circuit on output side during conduction interval

$$Q_\ell = \frac{\pi}{2}\,n = \frac{\pi}{4}\frac{R_{eff}}{Z_o} \therefore R_{eff} = 2n\ Z_o$$

R', the steady state input resistance is assumed to exist at only one frequency (where $\ell \simeq \lambda/4$ long). It is

$$R' = \frac{Z_o}{2n} \qquad (17)$$

The power output is then calculated by knowing the c_n from the Fourier Spectrum of the comb generating circuit. The Fourier Spectrum is

$$e_n = \sum_{n=-\infty}^{\infty} \frac{c_n}{2}\ e\ jn\omega_i t \qquad (18)$$

where $$c_n = \left(\frac{2E_p}{\pi N}\right)\frac{\cos \pi/2\ x}{1-x^2} = c_o\frac{\cos(\pi/2)\,x}{1-x^2} \qquad (19)$$

$$c_o = \frac{2E_p}{\pi N} \qquad (20)$$

E_p = peak pulse height of impulse generator
N = $1/(2f_{in}t_p)$
t_p = pulse width
ζ = $(1/2Z_0)\sqrt{L/c_{VR}}$; the damping factor of the impulse generator.

The power output is only in the nth harmonic; it is given by

$$P_n = \frac{C_n^2}{2R'}\frac{1}{\left(1+\dfrac{R_S}{R}\right)^2} \qquad (21)$$

where $$\begin{cases} Z_0 = \dfrac{t_p}{2\pi\ \zeta C_{VR}} \\ R' = Z_0/2n \end{cases}$$

The impulse power output is given by:

$$P_{impulse} = E_p^2/4NZ = \pi\zeta f_{in} C_{VR} E_p^2 \qquad (22)$$

where $\zeta = (1/2Z_o)\sqrt{L/C_{VR}}$, $t_p \cong \pi\sqrt{LC}$

Efficiency, as a ratio of *CW* output power to impulse power is:

P_n

$$\frac{P_n}{P_{imp}} = \frac{c_n^2 n\ (1/1 + R_S/R')^2}{Z_o \qquad \pi\zeta f_{in} C\ E_p^2}$$

$$\xi_{imp\to CW} = \left[\frac{4}{\pi}\cdot\frac{x\cos(\pi/2\ x)}{1-x^2}\cdot\frac{1}{1+\dfrac{2R_S}{Z_o}}\right]^2 x\ 100\%$$

where $$x = 2f_o t_p$$

APPENDIX B

Curves of Optimized Design Parameters

The efficiency calculations of Appendix A were programmed into a computer. The program was designed so that a pulse width could be formed giving optimum overall efficiency. It was expected that, while impulse to CW conversion would be best if the pulse were a half cycle wide at f_o, the overall efficiency might be higher with a wider pulse, since the efficiency of generating a wider pulse would be so much higher. The detailed computer calculations showed this to be the case.

The curves of efficiency, Figures 12 and 13, are results of this program. It should be emphasized that these are the efficiencies to a "damped waveform" output. CW output efficiency is obtained by multiplying ξ_0 or $\xi_{imp} \rightarrow$ CW by 0.63. This factor includes 0.8 dB filter loss and the 76% factor due to $Q_{\mathcal{L}} = \pi/2\,n$.

$$\text{CW efficiency} \simeq 0.63\ \xi_o$$

$$\xi_o = \text{damped waveform efficiency}$$

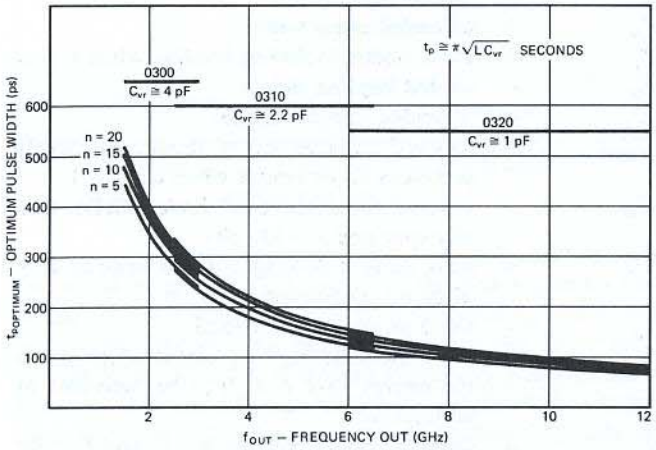

Figure B1. Optimum pulsewidth as a function of n and output frequency

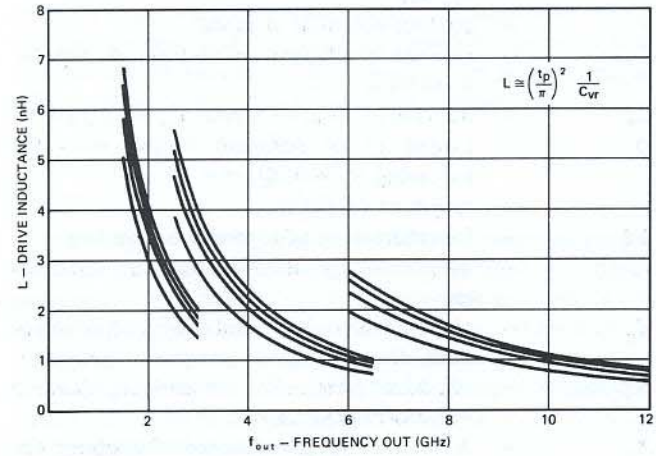

Figure B2. Required drive inductance for optimum pulsewidth

The optimum pulse width, upon which the efficiencies of Figures 13 and 14 are based, is given in Figure B1 for each of the HP diodes 0300, 0310, and 0320. Figures B2, B3, B4, and B5 give the required values of L, L_m, C_m, and C_T, to realize the required impulse.

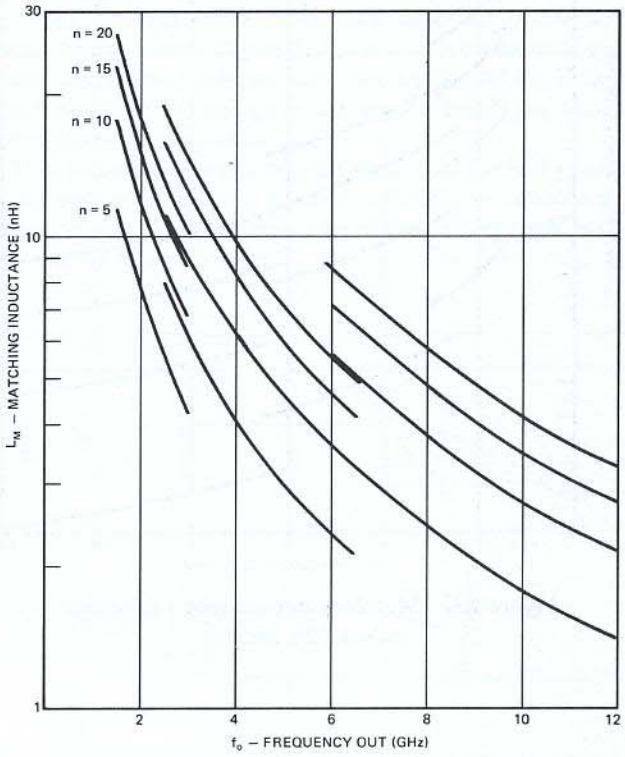

Figure B3. Matching inductance – optimum pulsewidth design

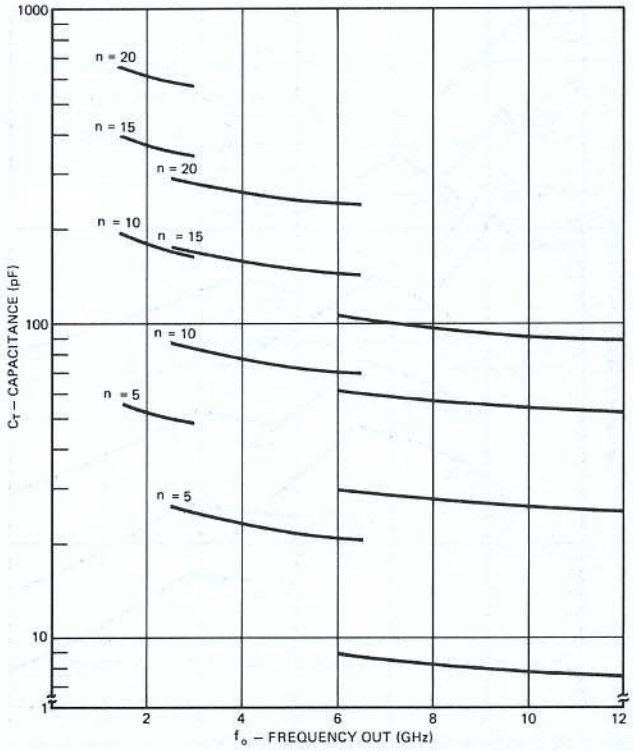

Figure B4. Tuning capacitance – optimum pulsewidth design

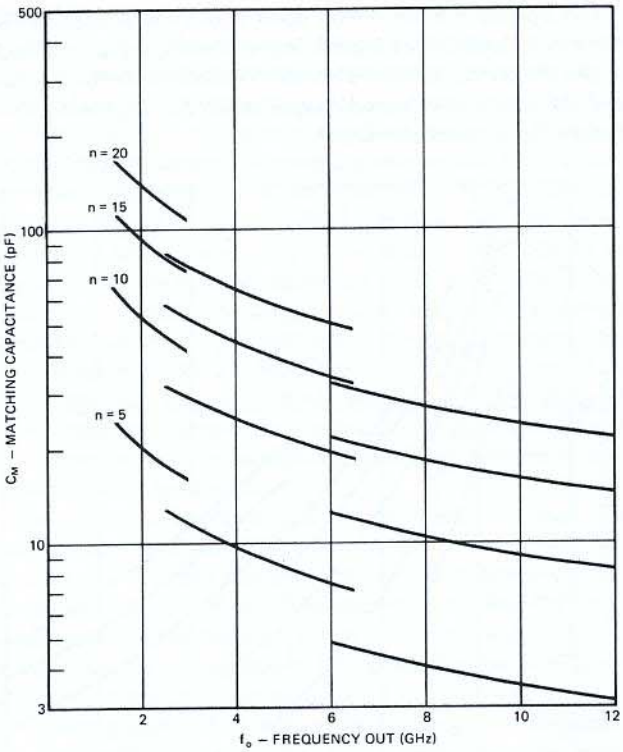

Figure B5. Matching capacitance – optimum pulsewidth design

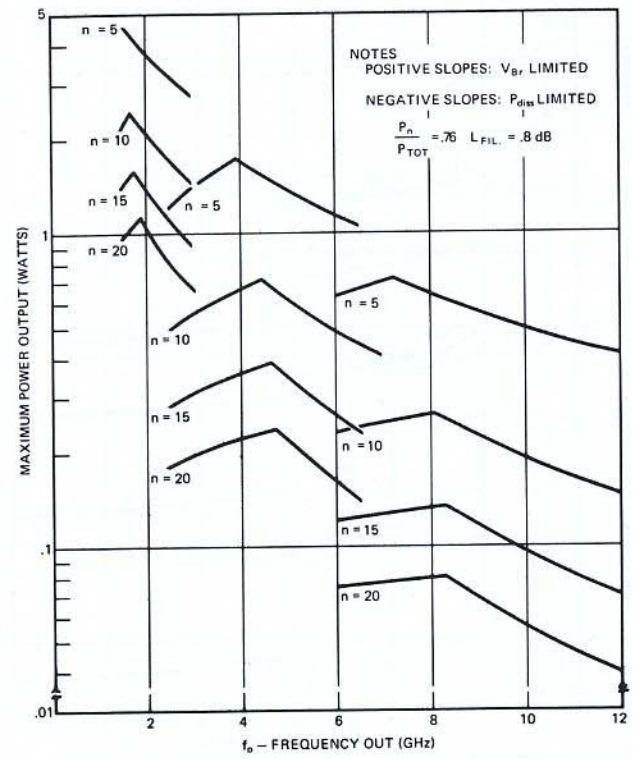

Figure B6. Maximum power output – optimum pulsewidth design

Power Output

The maximum power output from each of the HP diodes (0300, 0310, 0320) is shown in Figure B6. The power output is limited by either

a) the breakdown of the diode, or

b) the maximum dissipation of the diode.

The discontinuity in the curves of Figure B6 is due to the change in the limiting factor (a) to (b) with increasing f_o. The limitation due to maximum dissipation has a negative slope; the limitation due to breakdown has a positive slope in Figure B6.

SYMBOL DEFINITIONS

f_i	–	input frequency (Hz)
f_o	–	output frequency (Hz)
T_i, T_o	–	input, output periods
n	–	harmonic number, integral multiple of f_i
N	–	compression factor, related to pulse width, $N = 1/(2 f_i t_p)$
t_p	–	loaded pulse width
t'_p	–	unloaded pulse width
t''_p	–	pulse width, including loading when $t_t \neq o$
E_p	–	loaded impulse height
E'_p	–	unloaded impulse height
C_{Fwd}	–	forward capacitance of diode; effectively produces short circuit when $\omega\tau >> 1$
C_{vr}	–	reverse capacitance of diode (SRD), usually specified at −10 volts
I'_p	–	peak current flowing in L just prior to snap of diode (Unloaded: $R_L = \infty$)
I_p	–	same as above but loaded
L	–	drive inductance, the element which stores the energy ($1/2\ L\ I'^2_p$) to be delivered as an impulse
ζ	–	damping factor, relates R_L, L, and C_{vr}; for good impulse formation $\zeta < 0.5$
E	–	peak input voltage
V_o	–	output voltage, impulse generator output voltage.
0	–	contact potential of diode
C_n	–	Fourier coefficient of voltage of impulse waveform
C_o	–	dc term of Fourier series; $C_o = 2E_p/\pi N$
Q	–	loaded Q of resonant output network, assuming $R_S = 0$; $Q_u = \infty$
ℓ	–	length of output line
$\Delta\ell$	–	foreshortening of resonant output line
v_n	–	output voltage, damped waveform generator
Z_o	–	characteristic impedance of output resonant line, damped waveform generator
R_{eff}	–	effective terminating resistance, damped waveform generator
X_c	–	$X_c = 1/2\pi f_o C_c$; reactance of coupling capacitor, damped waveform generator
λ_o	–	output wavelength

R' – steady state input resistance (at f_o) of resonant output network when $Q_l \simeq \pi/2\ n$

R_{in} – input resistance (at terminals of C_T of impulse generator at f_i

C_n, L_N – damped element resonant output network elements

V_{BR} – diode breakdown voltage

R_S – diode series resistance

τ – effective minority carrier lifetime

t_t – transition time of the diode

L_p – package inductance

C_p – package capacitance

Θ_{jr} – thermal resistance of diode, °C/W

$P_{DISS_{MAX}}$ – maximum power at 25°C ambient; junction will be at maximum temperature

X_o – reactance of diode at f_0. $X_0 = 1/2\pi f_0 C_{VR}$

Efficiency Symbols

ξ_o – overall efficiency to damped waveform output. Assuming $Q = \pi/2\ n$ and 0.8 dB output filter loss, the total $CW \rightarrow CW$ efficiency would be $0.63\xi_o$

$\xi_{CW \rightarrow imp}$ – efficiency of producing an impulse

$\xi_{imp \rightarrow CW}$ – efficiency of converting impulse to damped waveform, $Q_\ell = \pi/2\ n$

P_{imp} – power in an impulse, watts; $\simeq \pi\zeta E_p^2 f_i C$

Impulse Generator Symbols

C_T – RF tuning capacitor, resonates out L at f_i

L_M, C_M – matching network

R_L – load resistance (50 Ω)

L_b, C_b, L_{CH} – bias tee elements

R_g – generator resistance (50 Ω)

R_b – bias resistance

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